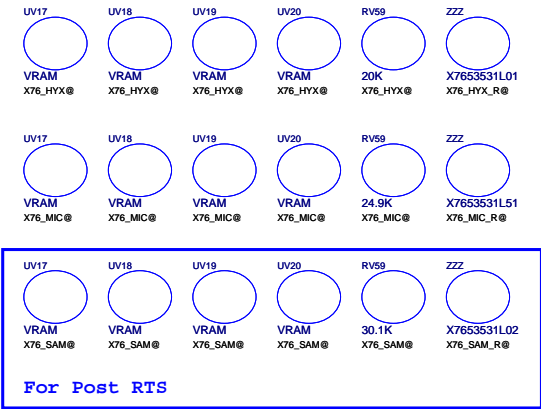


MODEL NAME : Marble Falls/ Discrete
PROJECT CODE : ZAL50, ZAL60
PCB NO : LA-B072P



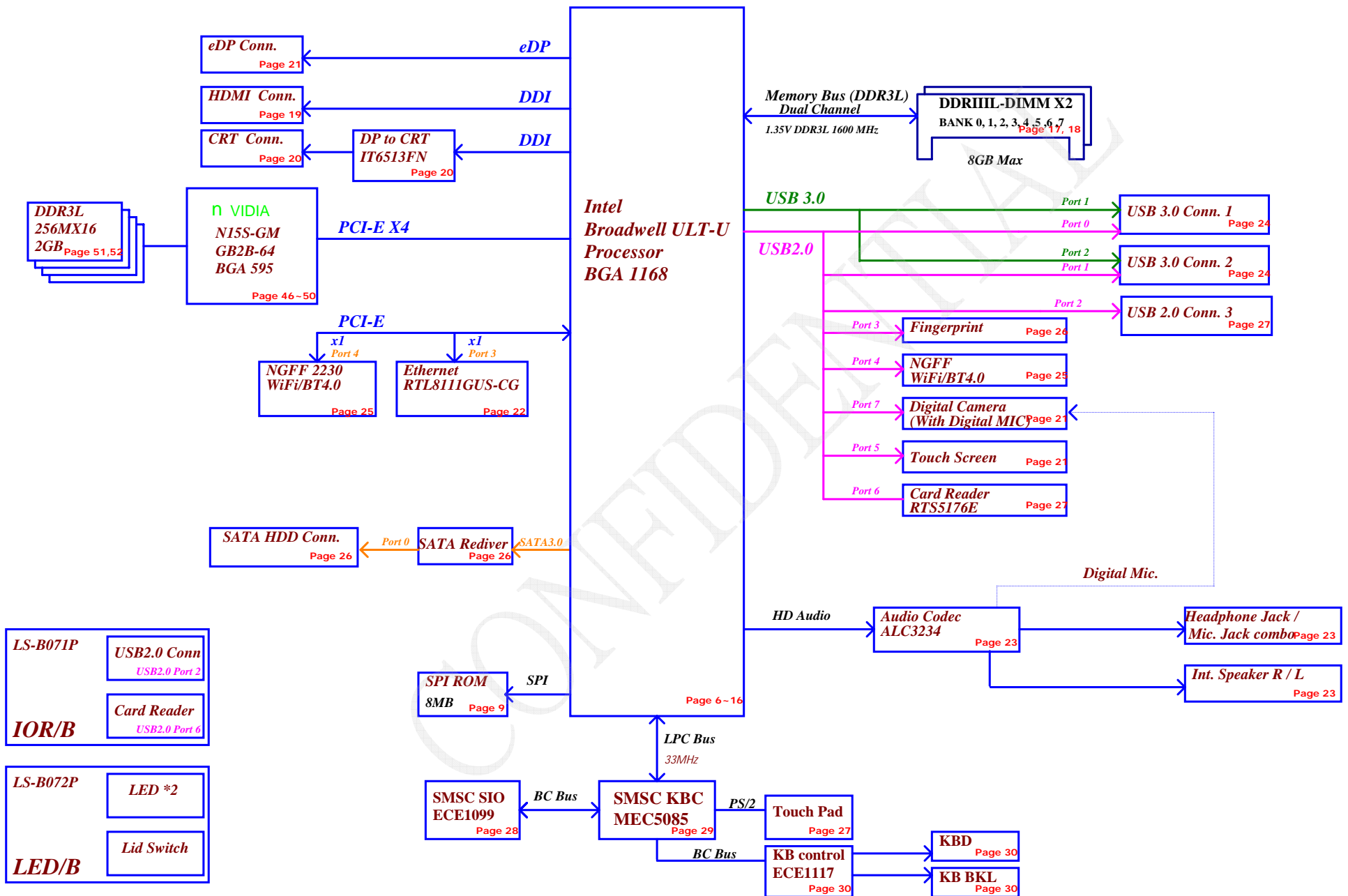
Dell / Compal Confidential

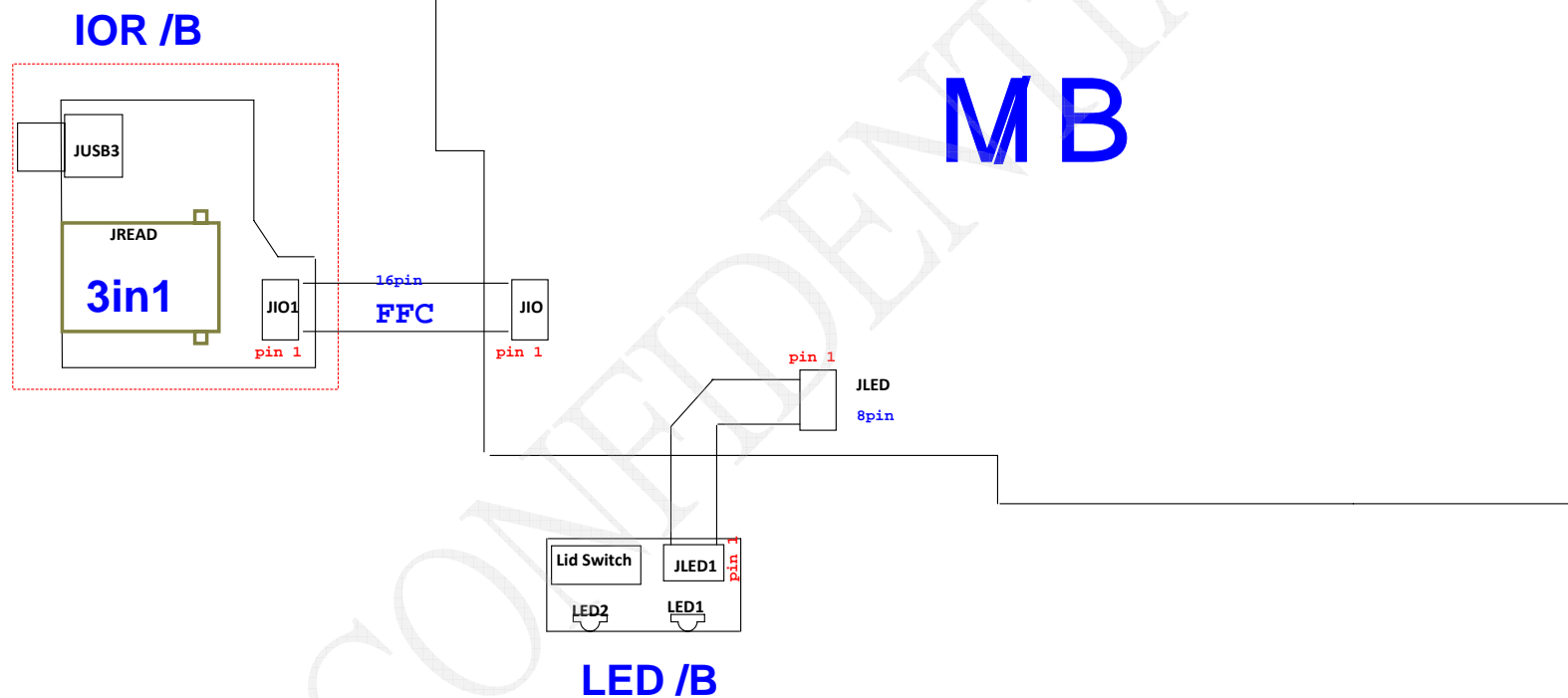
Schematic Document

Intel Broadwell ULT
Marble Falls 14"/15" Value
DIS

2013-10-03 Rev: 0.1

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Board ID Table

Phase ID

RE79	CE54	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	A00
4.3K	4700p	
2K	4700p	
1K	4700p	

BOARD ID rise time is measured from 5%~68%.

Config ID

RE89	RE90	Config
De-Pop	Pop	Discrete
Pop	De-Pop	UMA

SMBUS Control Table

	SOURCE	BATT	Charger	DDR3L	XDP	WLAN NGFF	Touch pad	VGA
CHARGER_SMBCLK CHARGER_SMBDAT	MEC5085		V					
PBAT_SMBCLK PBAT_SMBDAT	MEC5085	V						
GPU_SMBCLK GPU_SMBDAT	MEC5085							V
SML1_SMBCLK SML1_SMBDATA	MEC5085							
SMBCLK SMBDATA	ULT			V	V	V	V	
SML0CLK SML0DATA	ULT							
SML1CLK SML1DATA	ULT							

Link

CLOCK SIGNAL

CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100/1000 LAN
CLKOUT_PCIE3	NGFF (BT + WLAN)
CLKOUT_PCIE4	
CLKOUT_PCIE5	

Symbol Note :



: means Digital Ground



: means Analog Ground

ULT

USB3.0

Port1	USB connector 1
Port2	USB connector 2
Port3	
Port4	

USB2.0

Port0	USB connector 1
Port1	USB connector 2
Port2	USB connector 3 (IO/B)
Port3	Finger print
Port4	NGFF (BT + WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera

PCI EXPRESS

Lane 1	
Lane 2	
Lane 3	10/100/1000 LAN
Lane 4	NGFF (BT + WLAN)
Lane 5	PEG (N15S)
Lane 6	

SATA

SATA0	HDD
SATA1	
SATA2	
SATA3	

DDI

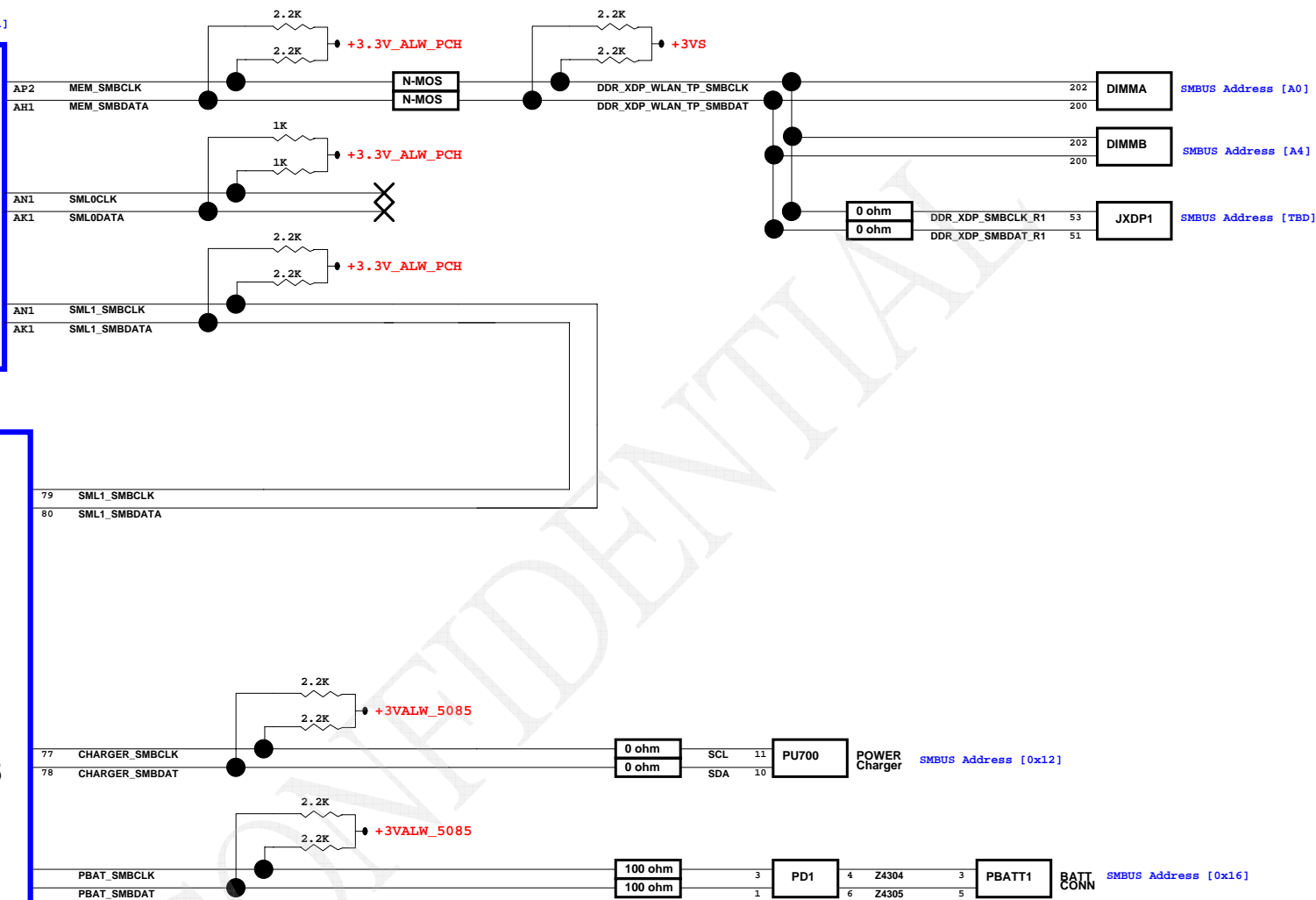
DDI1	HDMI
DDI2	DP to CRT

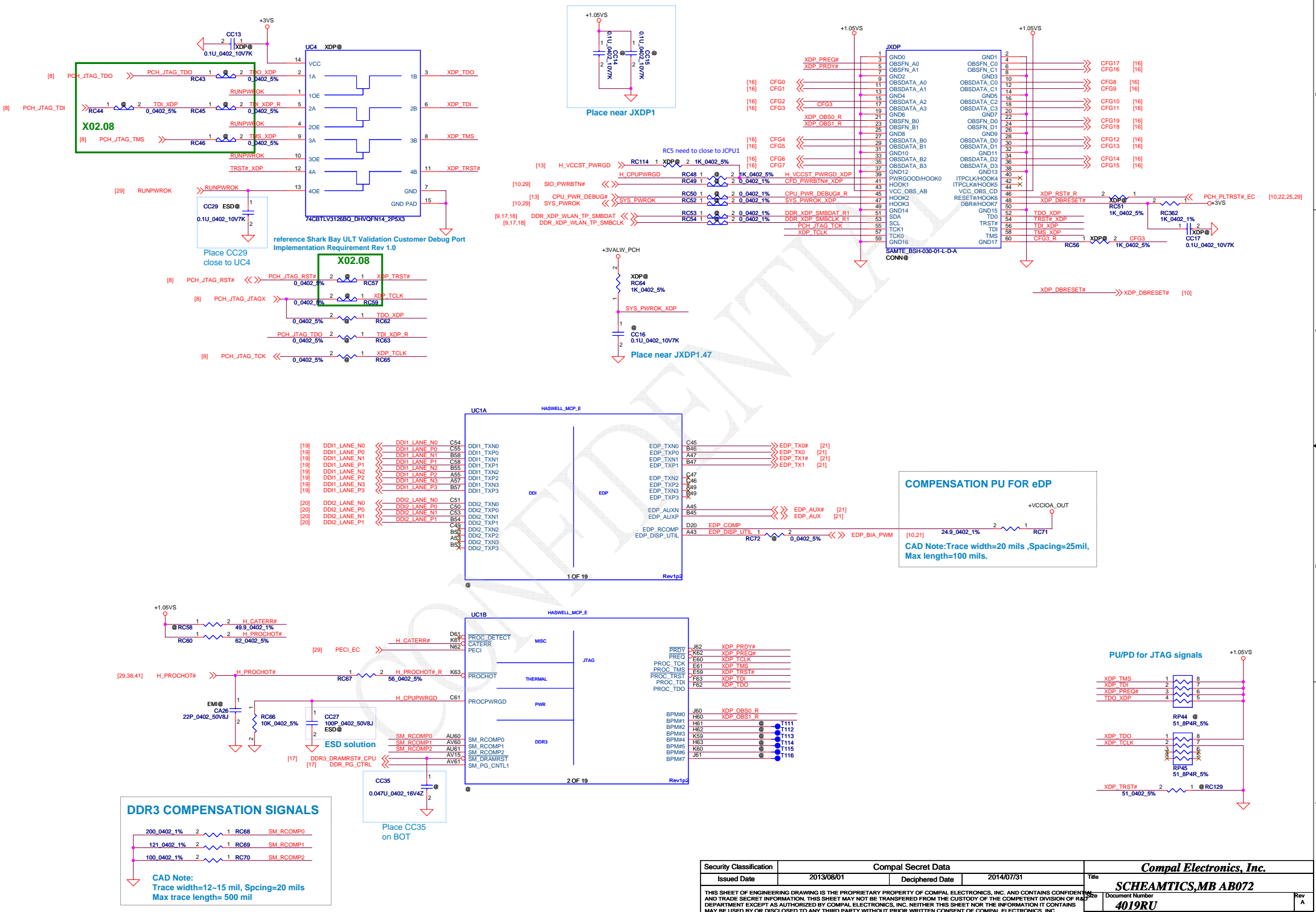
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SMBUS Address [0x9a]

MCP

MEC 5085





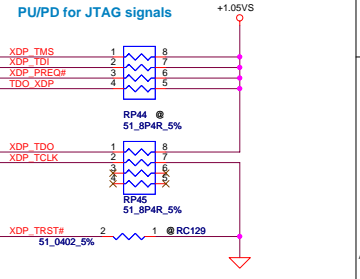
DDR3 COMPENSATION SIGNALS

200_0402_1% 2 1 RC68 SM_RCOMP0
121_0402_1% 2 1 RC69 SM_RCOMP1
100_0402_1% 2 1 RC70 SM_RCOMP2

CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

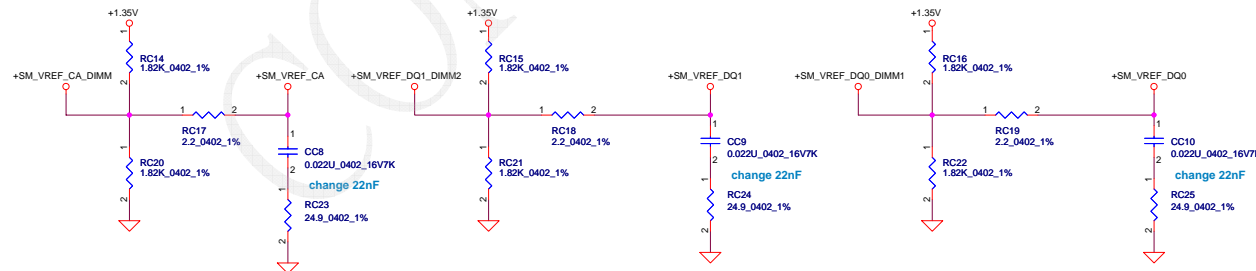
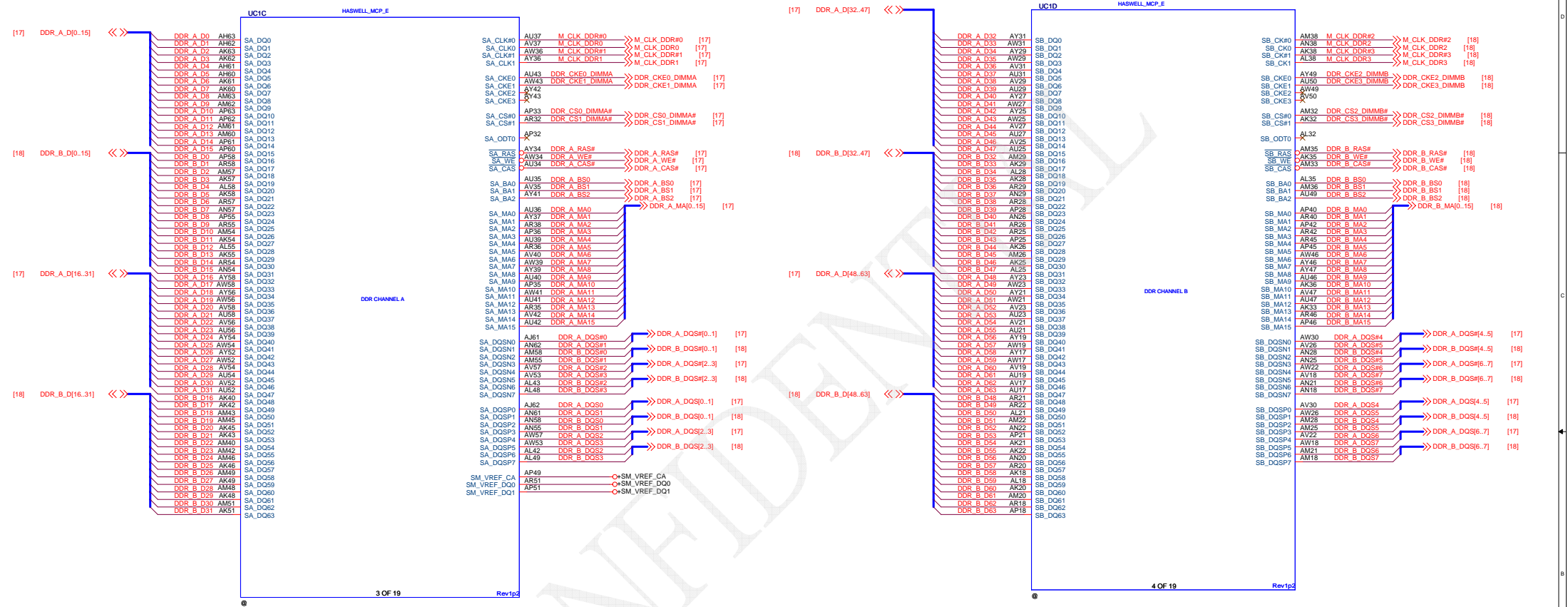
COMPENSATION PU FOR eDP

24.9_0402_1% 2 1 RC71
CAD Note:Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.



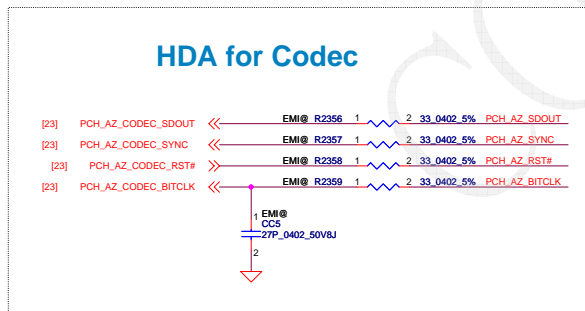
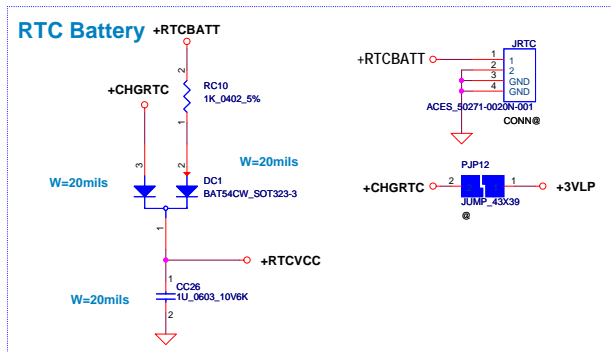
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Interleaved Memory

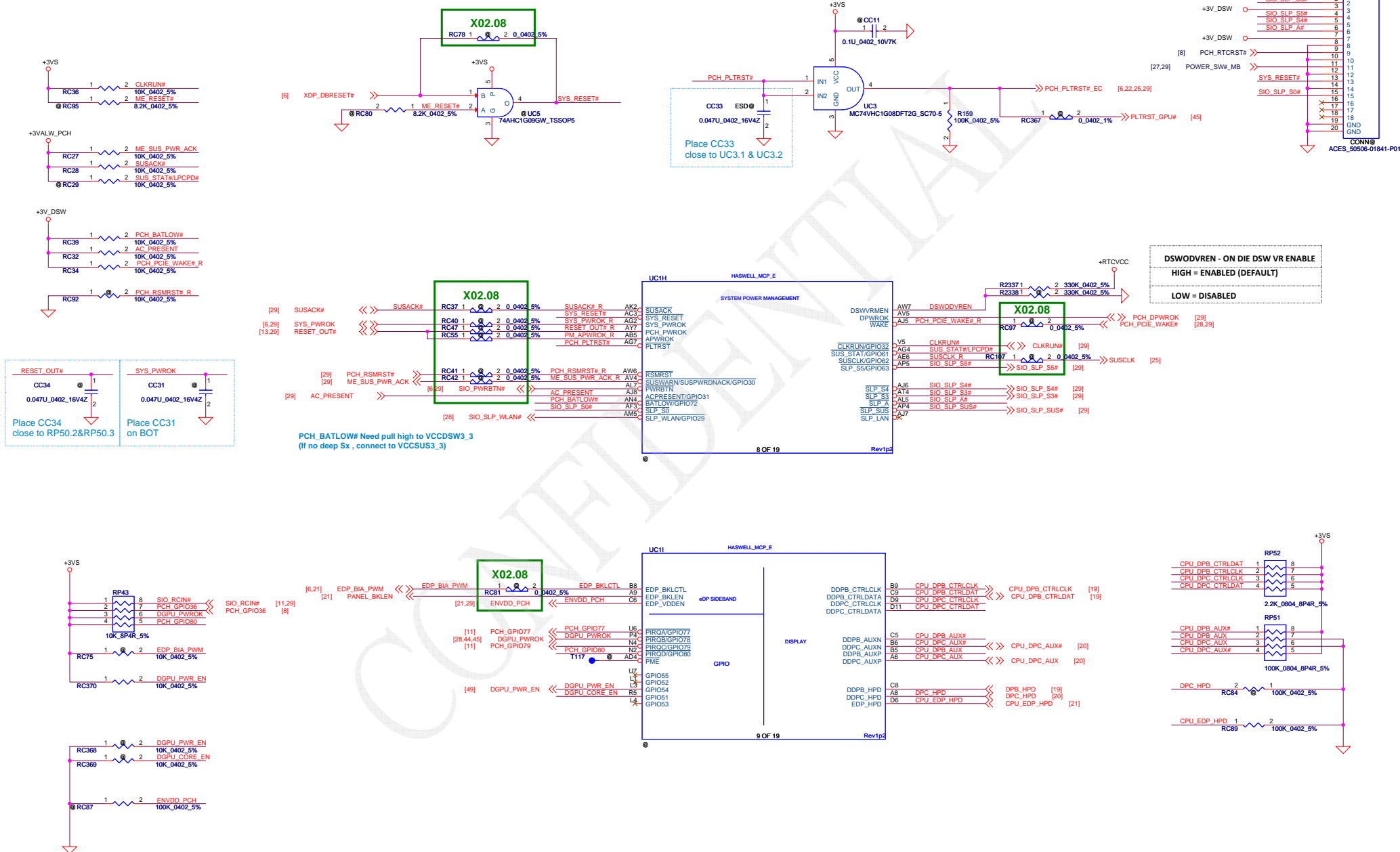


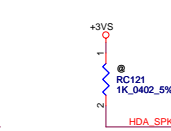
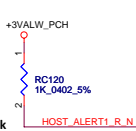
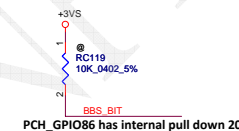
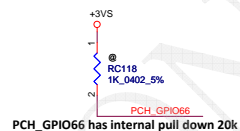
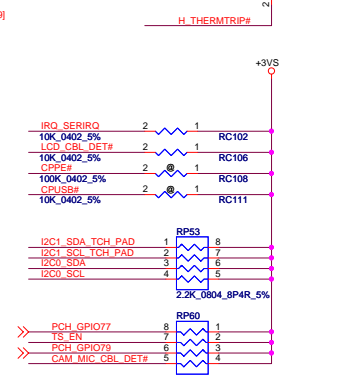
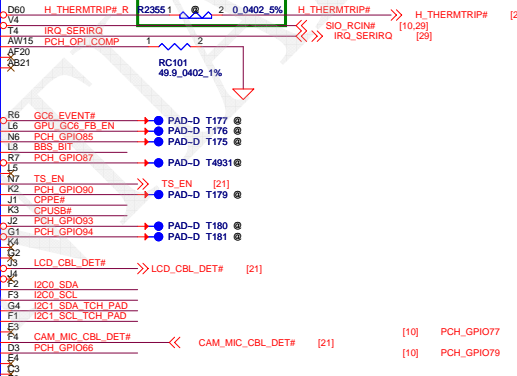
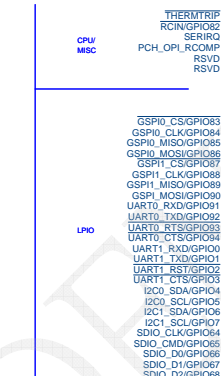
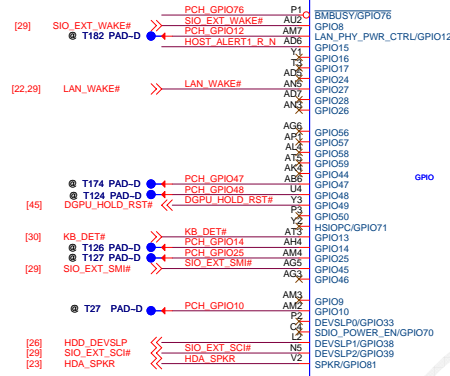
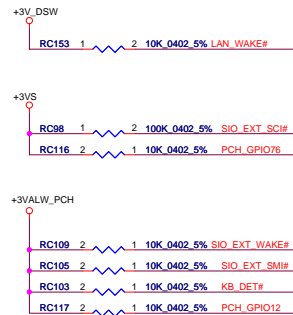
confirm by intel request PDG P141

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GPIO66
TOP-BLOCK SWAP OVERRIDE
HIGH depop RC118 (DEFAULT)
LOW pop RC122

GPIO86
BOOT BIOS STRAP BIT BBS
HIGH LOW(DEFAULT) LPC
LOW(DEFAULT) SPI

GPIO15
TLS CONFIDENTIALITY
HIGH LOW(DEFAULT)

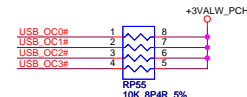
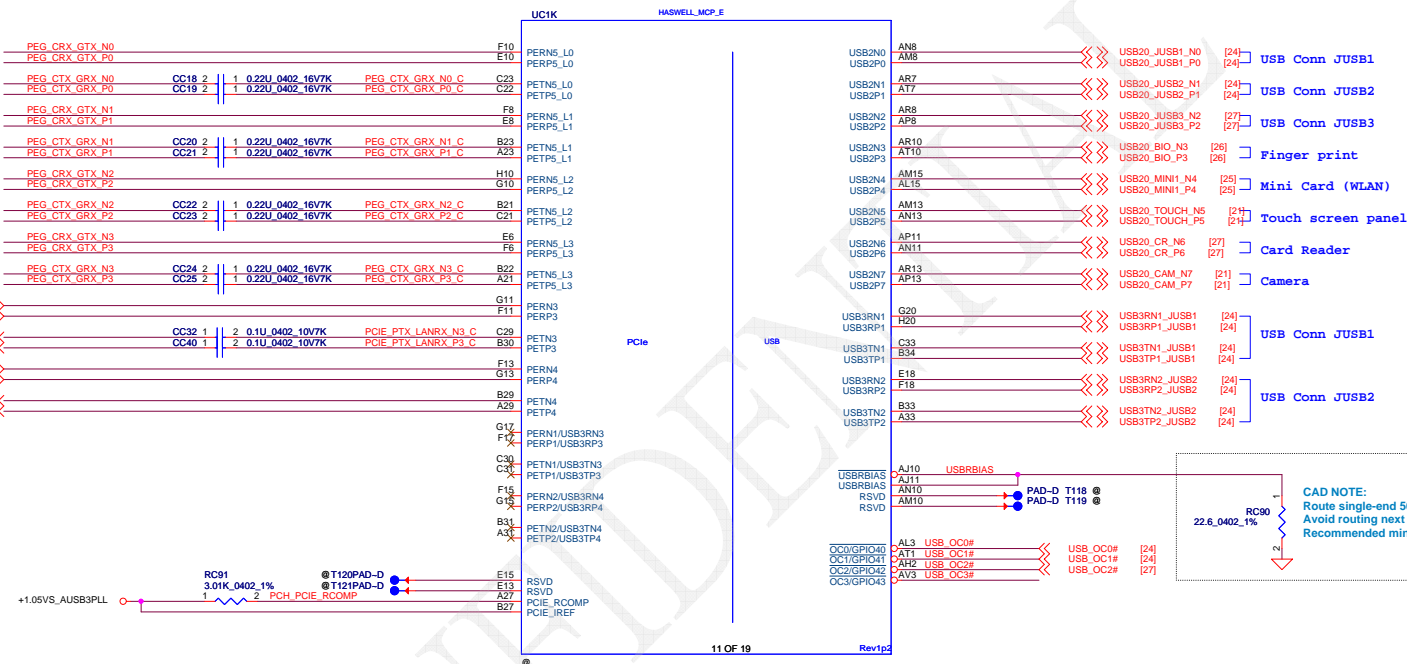
GPIO81
NO REBOOT STRAP
HIGH LOW(DEFAULT) disable
LOW(DEFAULT) enable

[45] PEG_CTX_GRX_P0[0..3] >> PEG_CTX_GRX_P0[0..3]
[45] PEG_CTX_GRX_N0[0..3] >> PEG_CTX_GRX_N0[0..3]
[45] PEG_CRX_GTX_P0[0..3] << PEG_CRX_GTX_P0[0..3]
[45] PEG_CRX_GTX_N0[0..3] << PEG_CRX_GTX_N0[0..3]

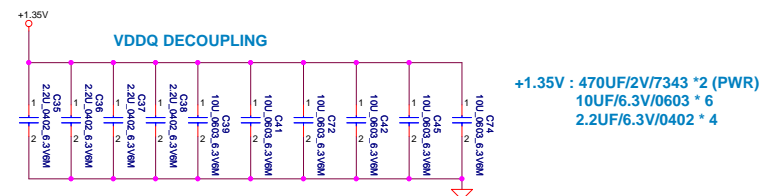
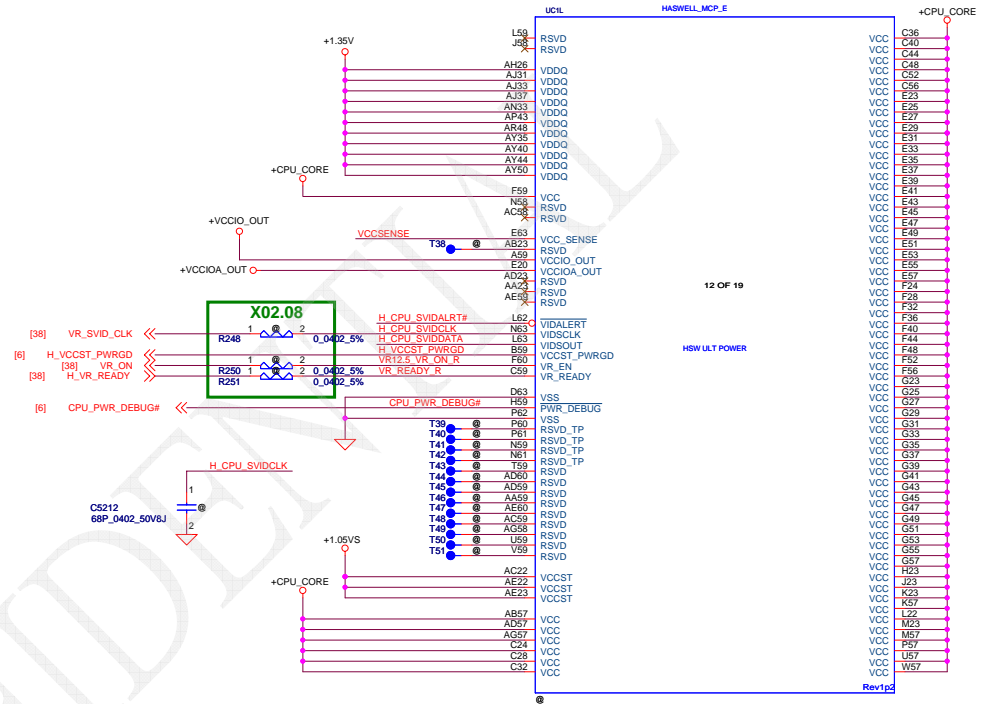
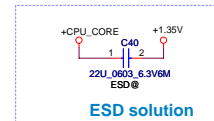
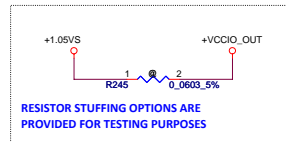
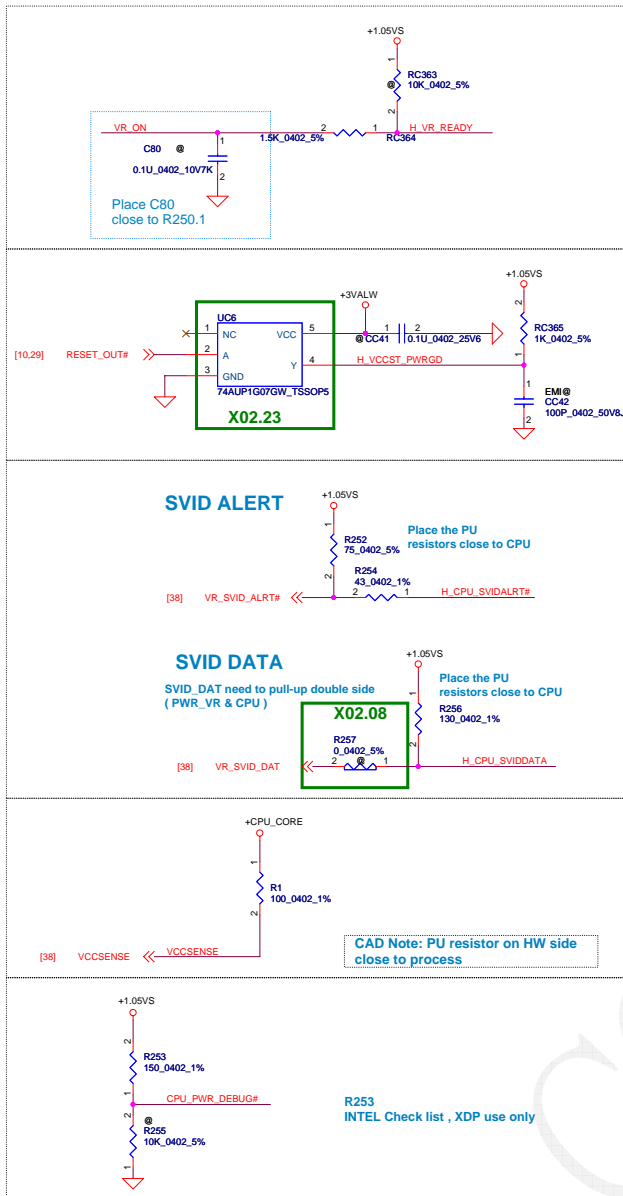
LAN

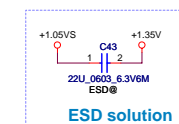
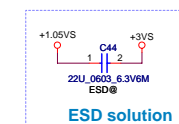
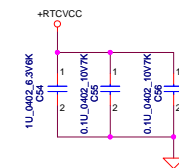
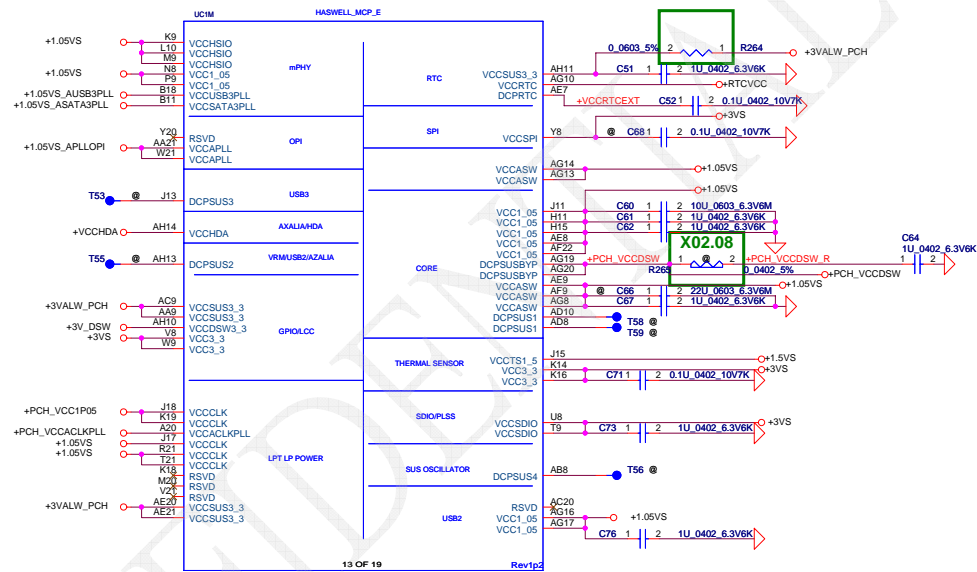
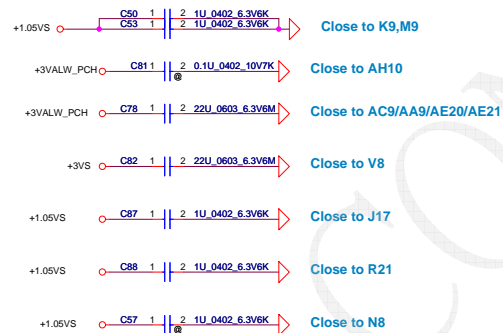
NGFF WLAN

[22] PCIE_PRX_LANTX_N3
[22] PCIE_PRX_LANTX_P3
[22] PCIE_PTX_LANRX_N3
[22] PCIE_PTX_LANRX_P3
[25] PCIE_PRX_WLANTX_N4
[25] PCIE_PRX_WLANTX_P4
[25] PCIE_PTX_WLANRX_N4
[25] PCIE_PTX_WLANRX_P4

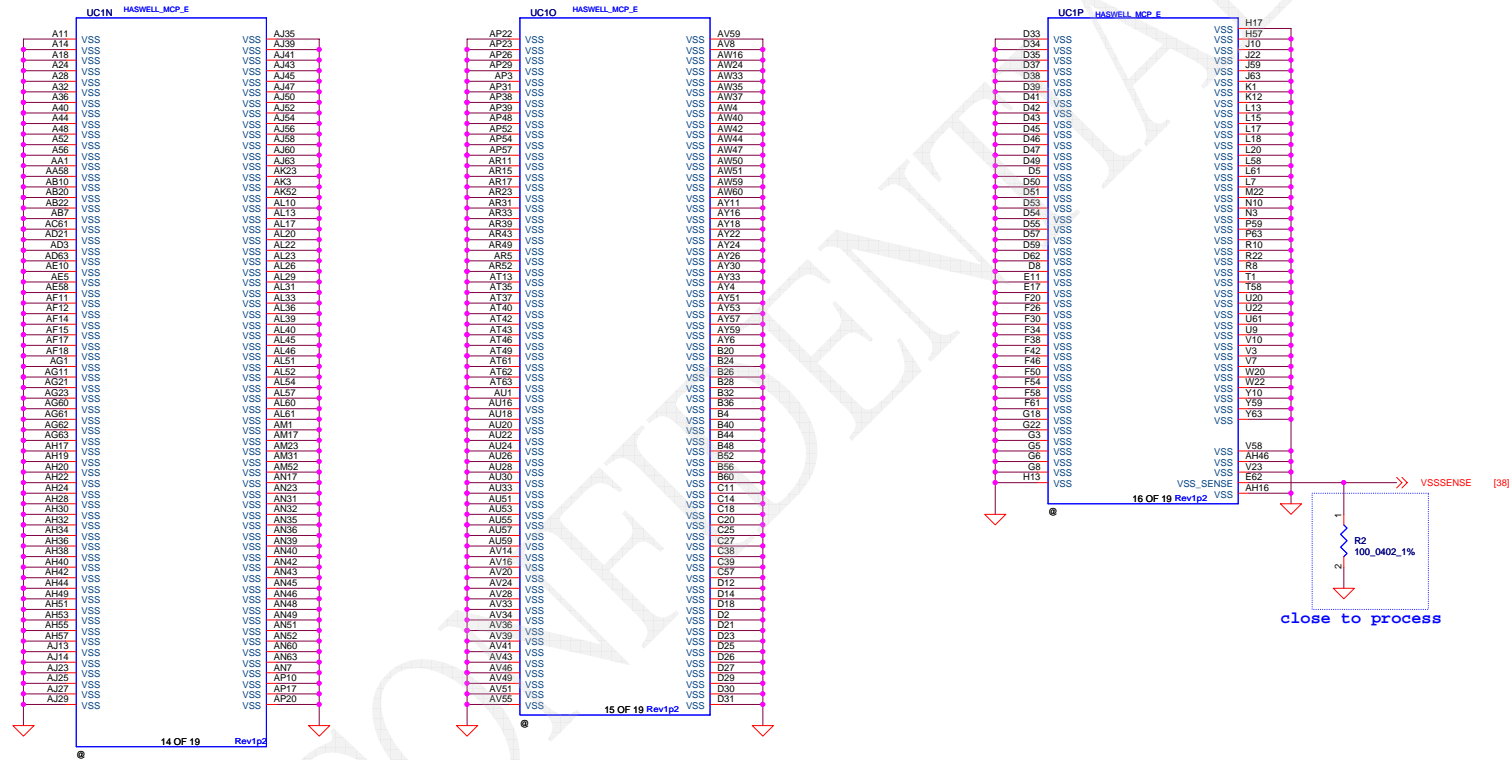


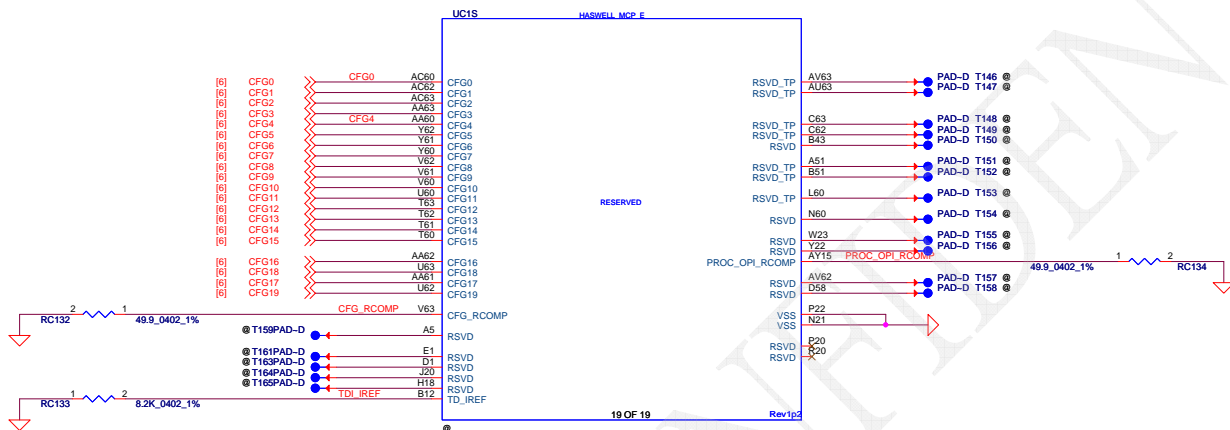
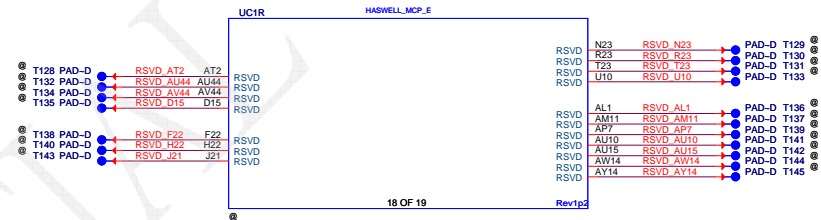
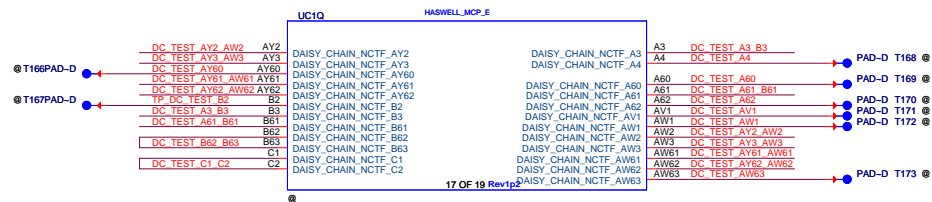
CAD NOTE:
Route single-end 50-ohms and max 500-mils length.
Avoid routing trace to clock pins or under stitching capacitors.
Recommended minimum spacing to other signal traces is 15 mils.





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CFG STRAPS for CPU



	Display Port Presence Strap
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



	EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

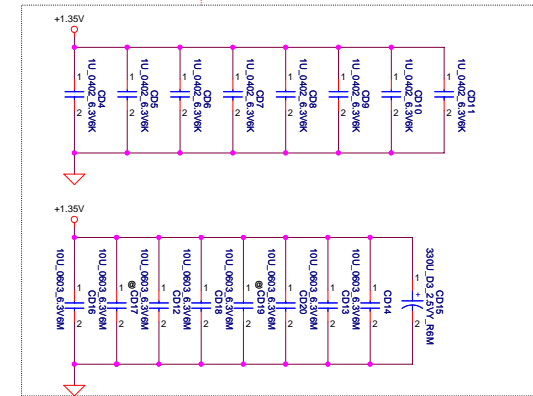
Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

[7] DDR_A_DQS[0..7] <<<
[7] DDR_A_D[0..63] <<<<
[7] DDR_A_DQS[0..7] <<<<
[7] DDR_A_MA[0..15] <<<<

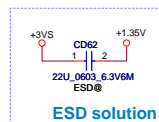
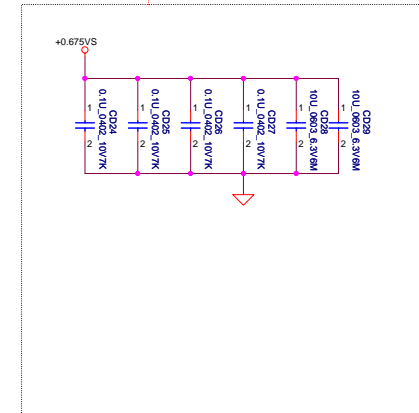
All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

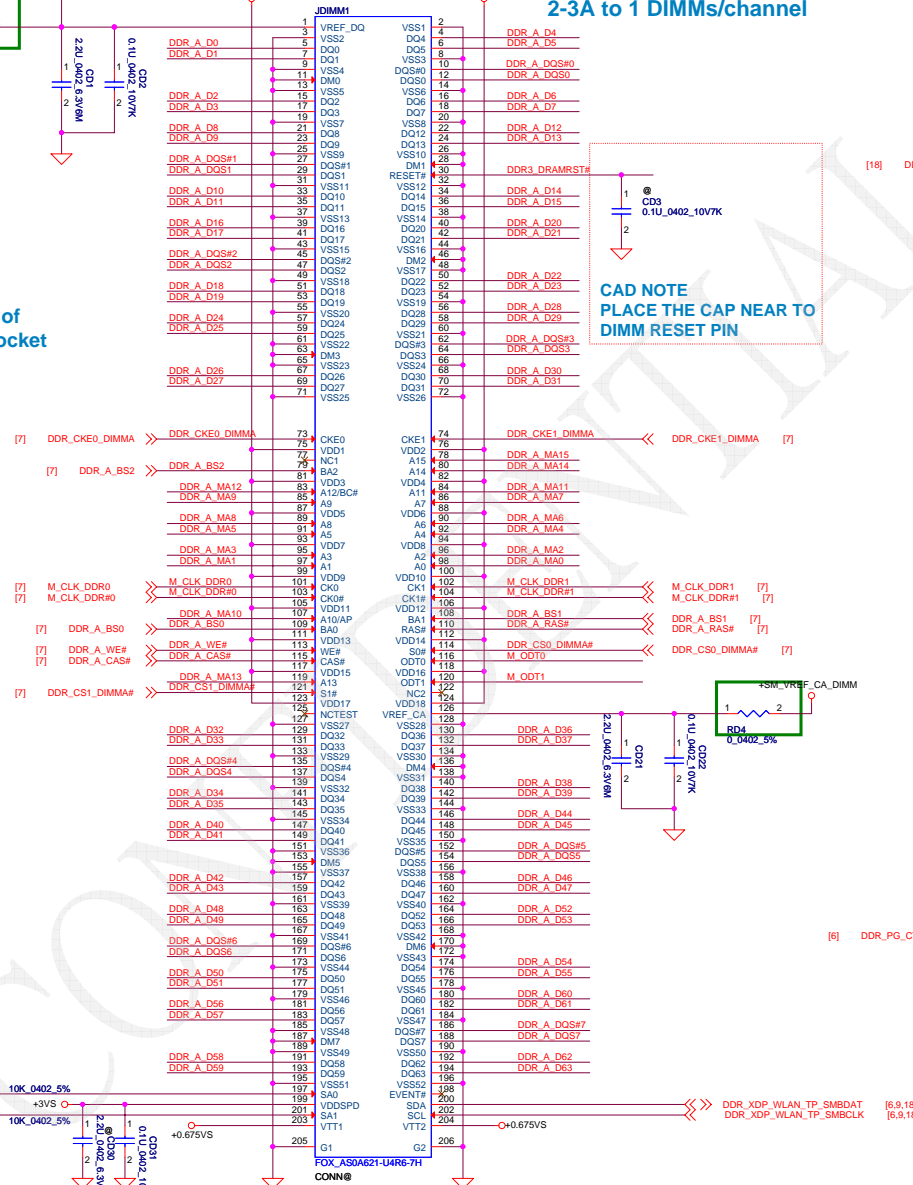


Layout Note:
Place near JDIMM1.203,204



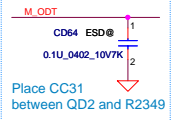
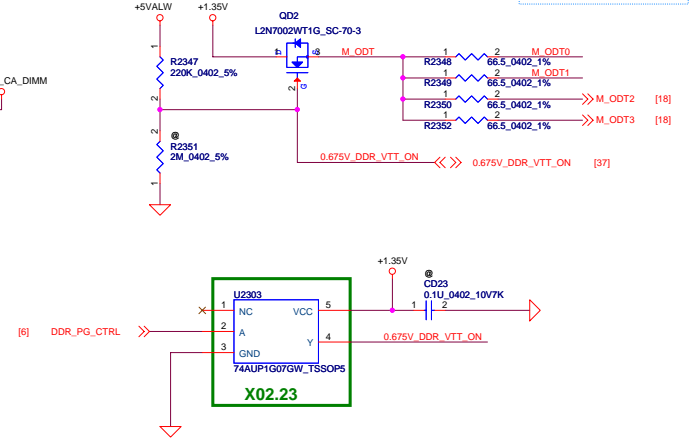
H=4mm

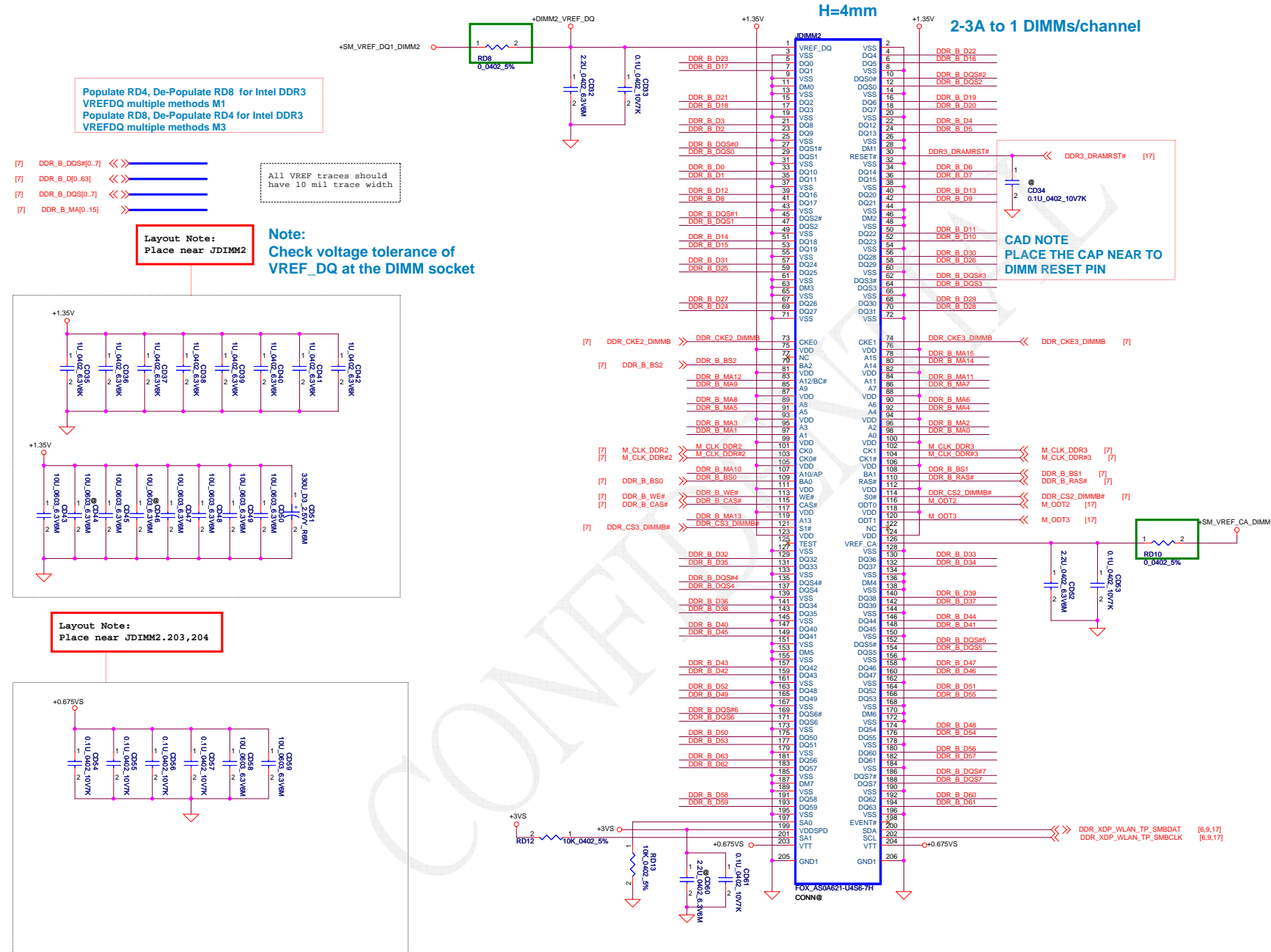
2-3A to 1 DIMMs/channel

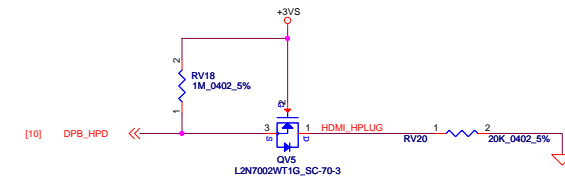
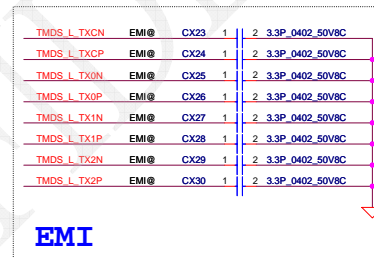
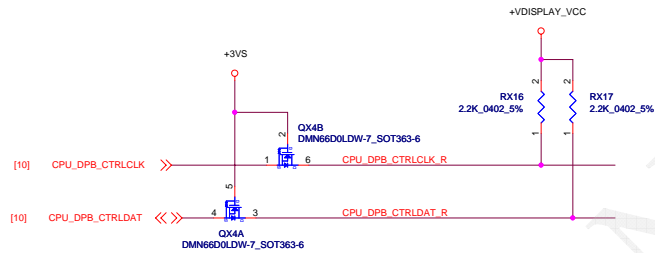
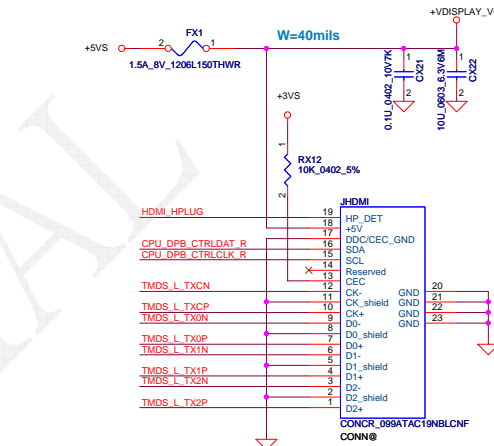
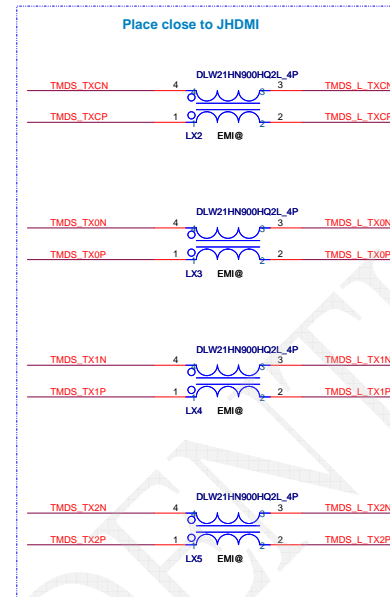
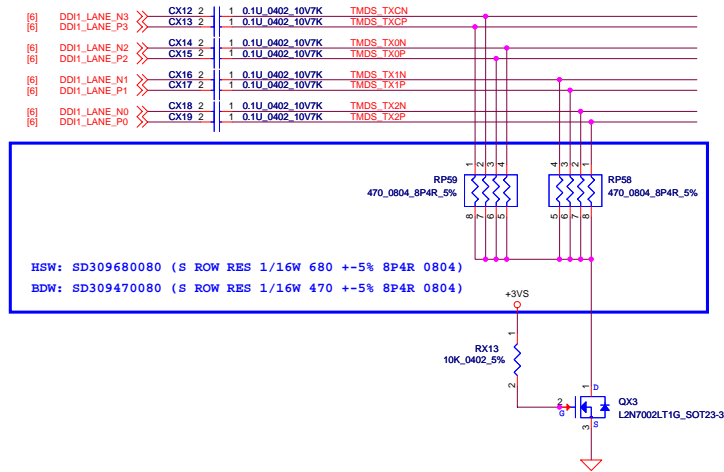


CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

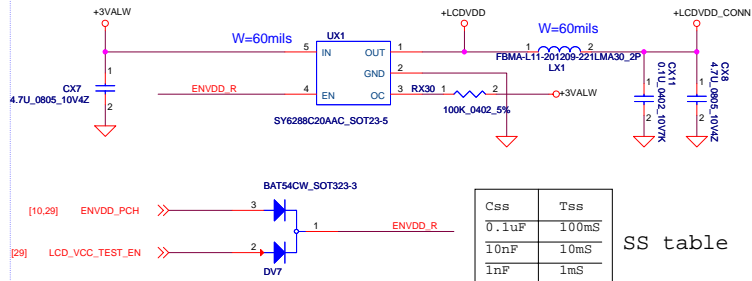
DDR3L SODIMM ODT GENERATION







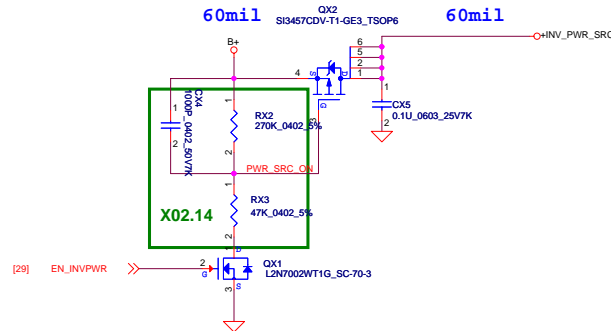
LCD PWR CTRL



Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

SS table

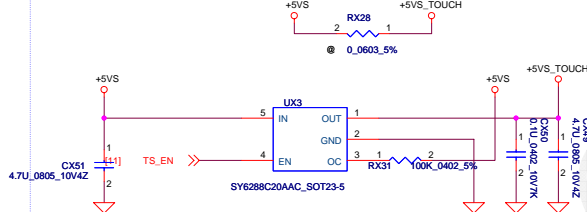
LCD backlight PWR CTRL



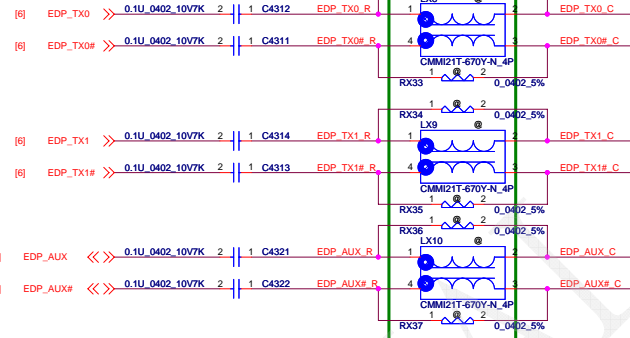
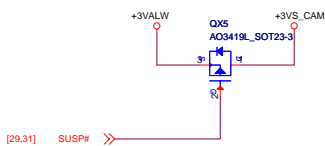
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

SS table

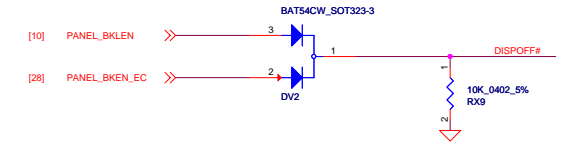
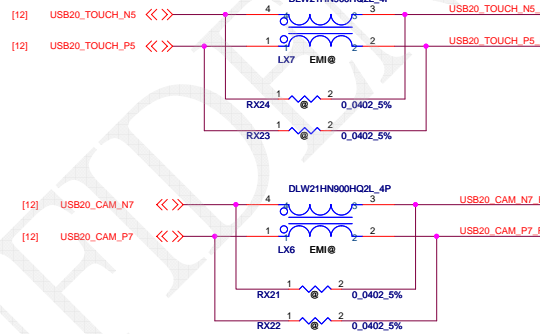
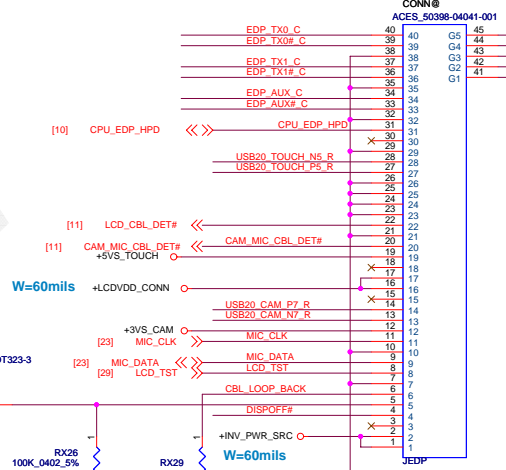
* Touch Screen Panel



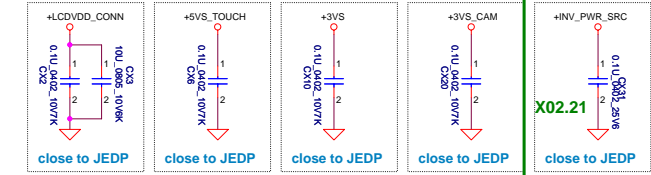
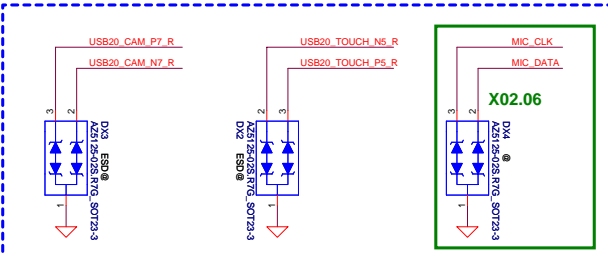
Webcam PWR CTRL



eDP Connector



close to JEDP

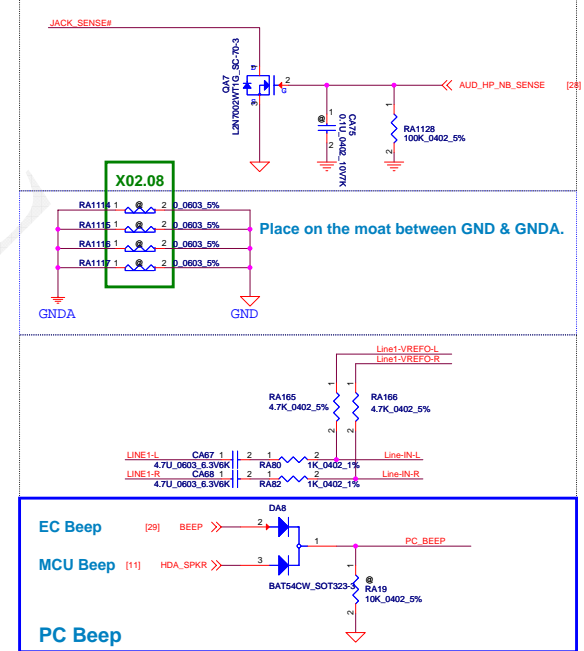
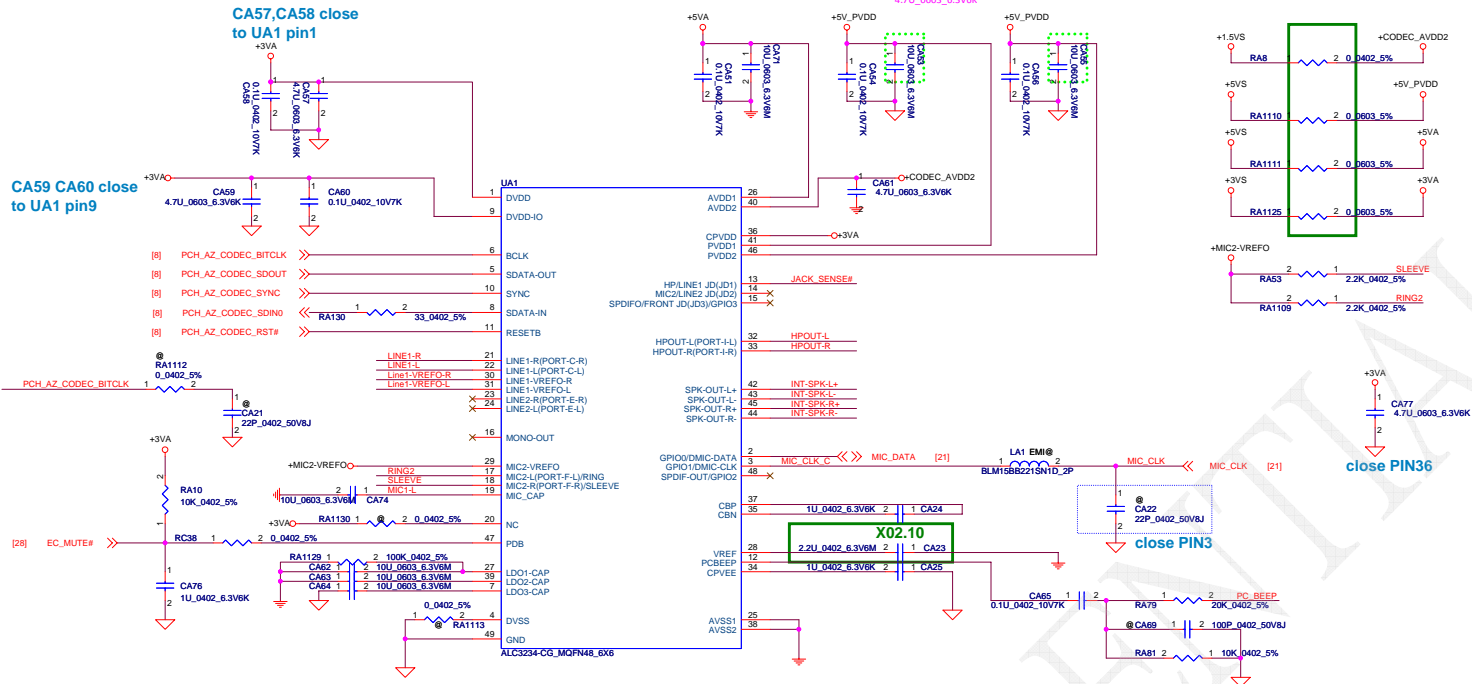


CA71, CA51 place close to Pin 26

CA3, CA55 change Value
from 10U_0603_6.3V6M to
4.7U_0603_6.3V6K

CA57,CA58 close
to UA1 pin1

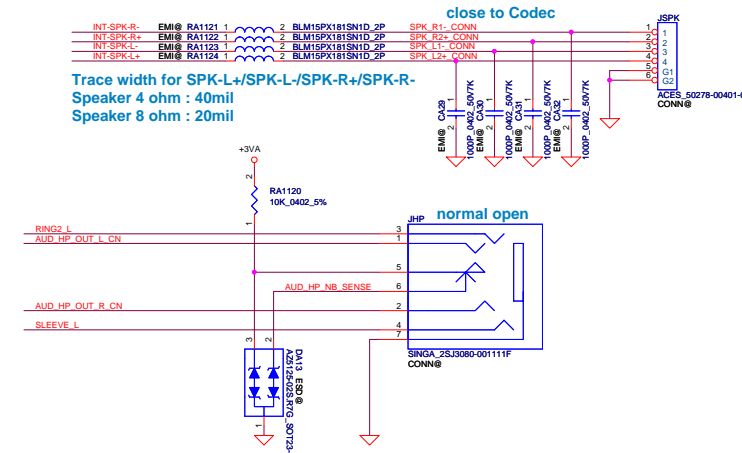
CA59 CA60 close
to UA1 pin9



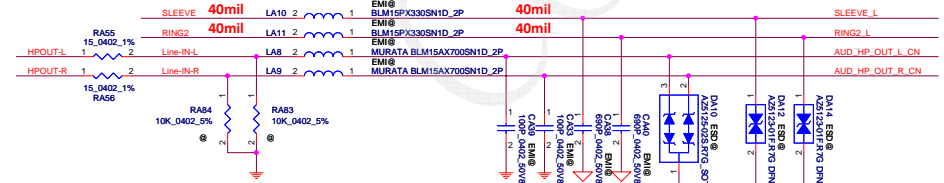
Close to UA1
Pin11,13,14,16

close to Codec

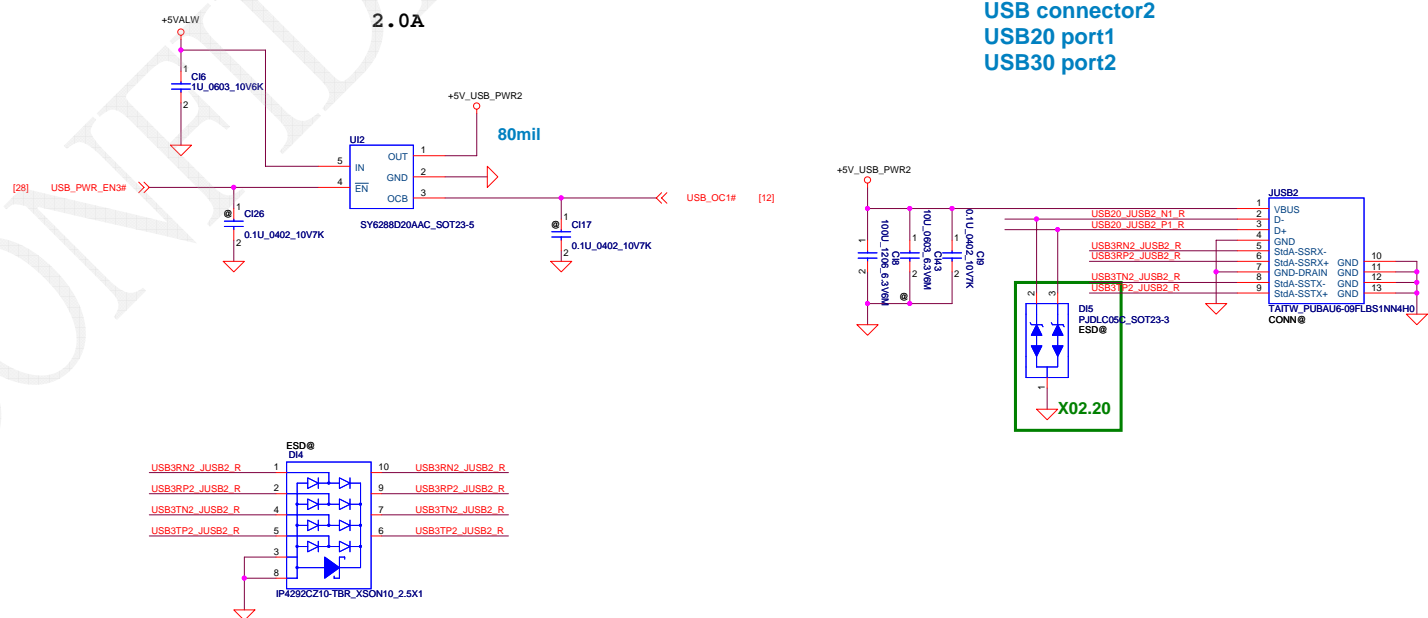
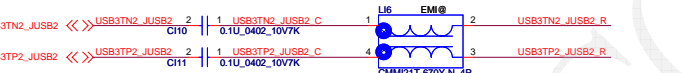
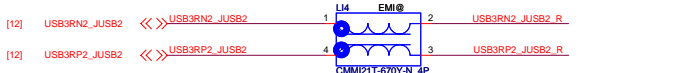
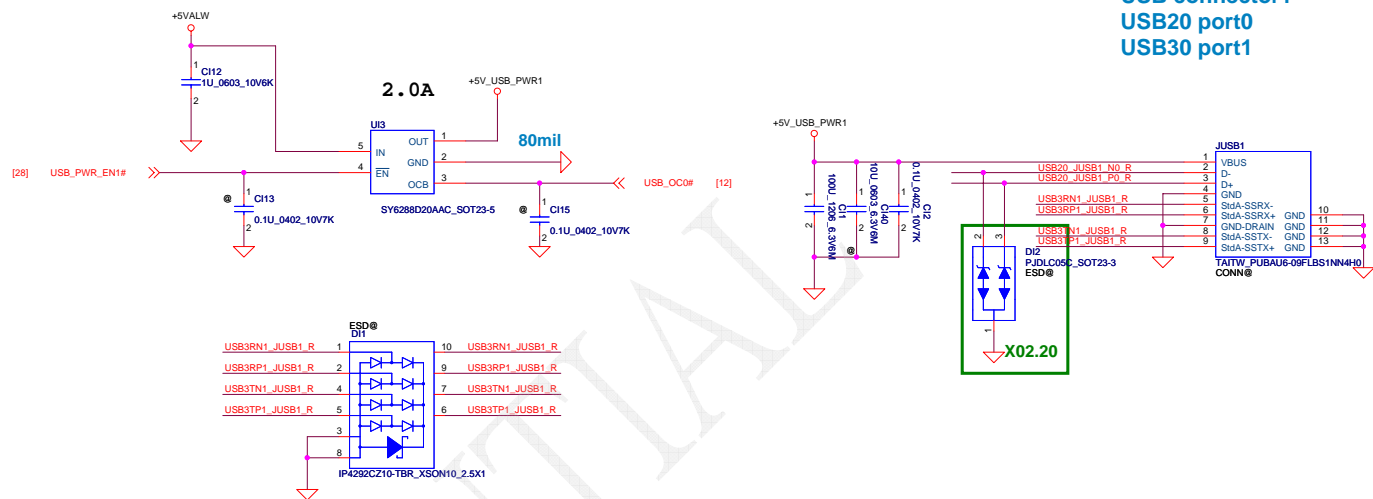
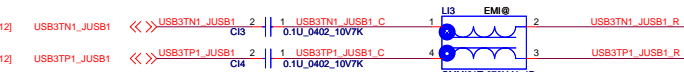
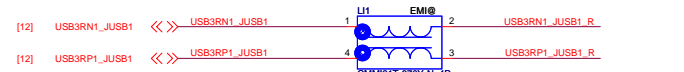
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil



iPhone and Nokia type Combo Jack

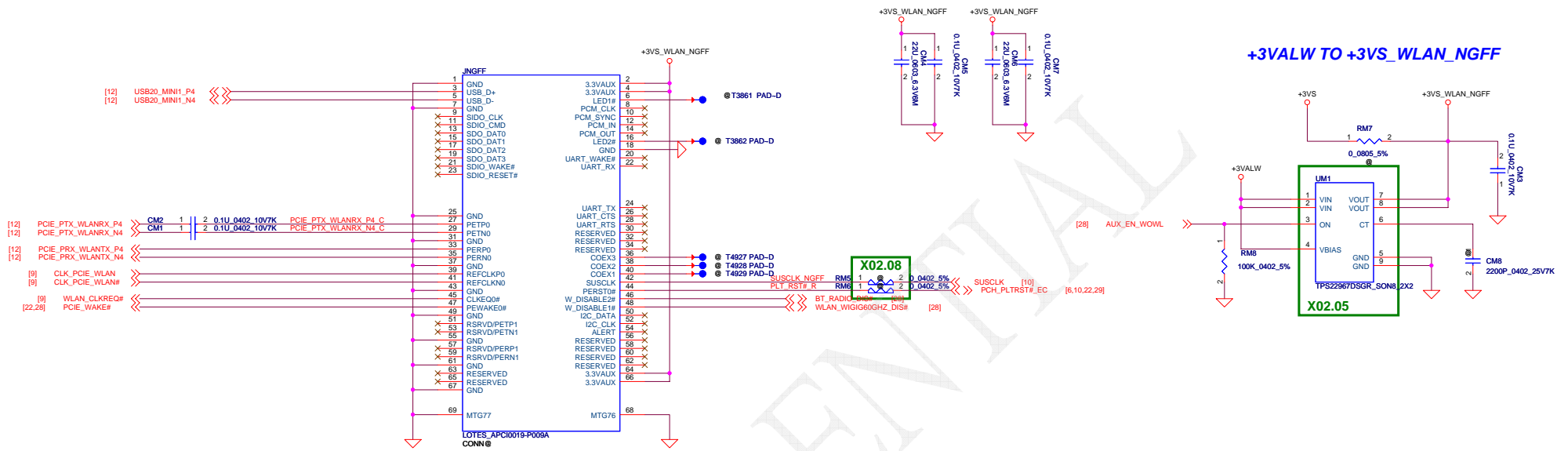


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closed to pin 2, 4 closed to pin 64, 66

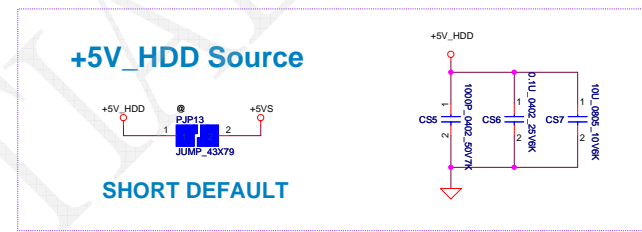
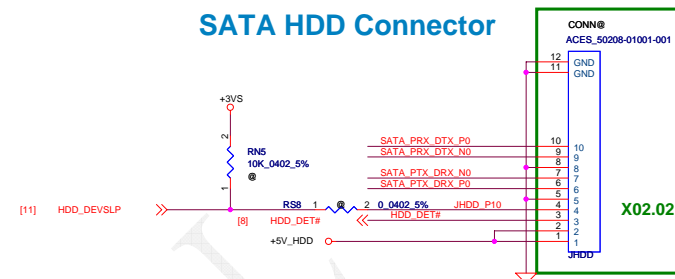
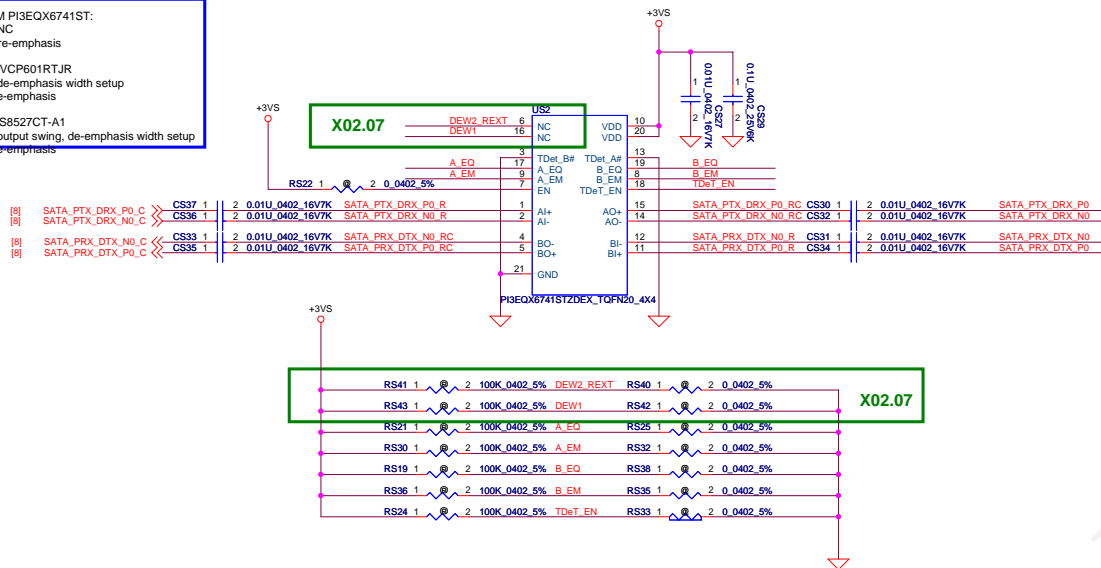


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PERICOM PI3EQX6741ST:
Pin6/16, NC
Pin8/9, Pre-emphasis

TI SN75LVCP601RTJR
Pin6/16, de-emphasis width setup
Pin8/9, de-emphasis

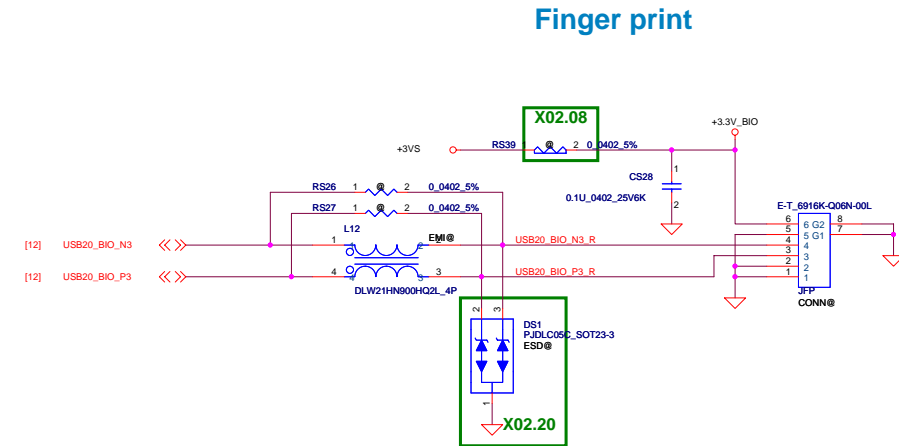
Parade PS8527CT-A1
Pin6/16, output swing, de-emphasis width setup
Pin8/9, de-emphasis

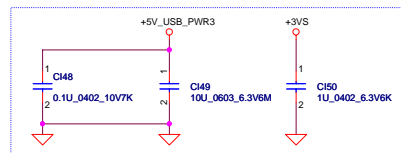
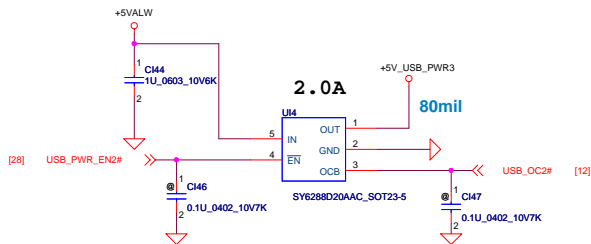


	DEW2	B_EM	A_EM	Tdet_A	DEW1	A_EQ	Tdet_EN	B_EQ
	PIN6	PIN8	PIN9	PIN13	PIN16	PIN17	PIN18	PIN19
Pericom PI3EQX6741ST	NC	PD (RS35)	NC (IP0)	PD	NC	NC	PH (RS24)	PD (RS38)
TI SN75LVCP601	NC (IP0)	PD (RS35)	PD (RS32)	PD	NC (IP0)	PD (RS25)	PD (RS33)	NC
Parade PS8527C	PD (RS40)	PD (RS35)	PH (RS30)	PD	NC	PD (RS25)	PD (RS33)	NC

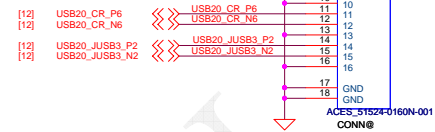
			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0 NC 1	3dB 6dB 9dB	3dB 6dB 9dB	0 NC 1	0dB 1.5dB	0dB 1.5dB
2nd	TI	0 NC 1	7dB 0dB 14dB	7dB 0dB 14dB	0 NC 1	0dB -6dB -3dB	0dB -6dB -3dB
3rd	Parade	EQ2 (M = VDD/2) 0 M 0 0 0 1 M M M 0 M 1 1 M 1 0 1 1	2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	0 M 1	0dB -3.5dB -1.5dB	0dB -3.5dB -1.5dB

* red color is current setting

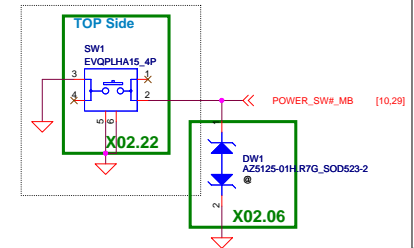




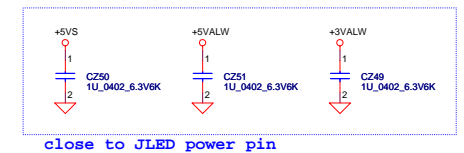
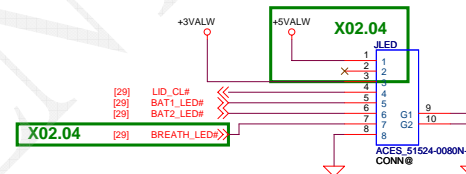
IO to MB CONN



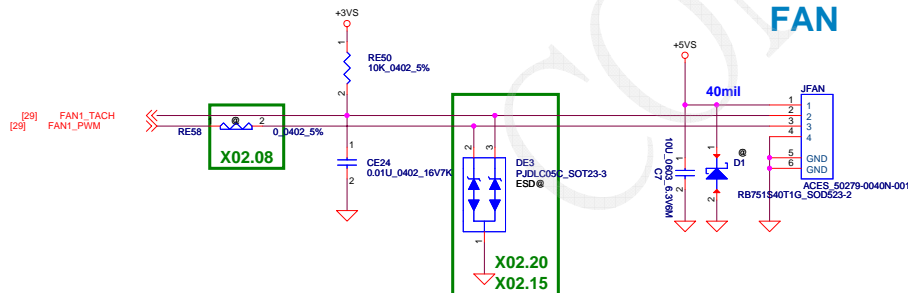
ON/OFF switch



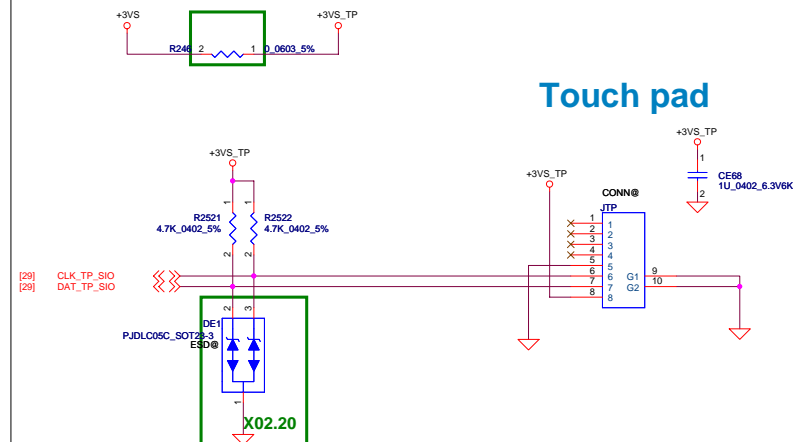
LED/B TO M/B



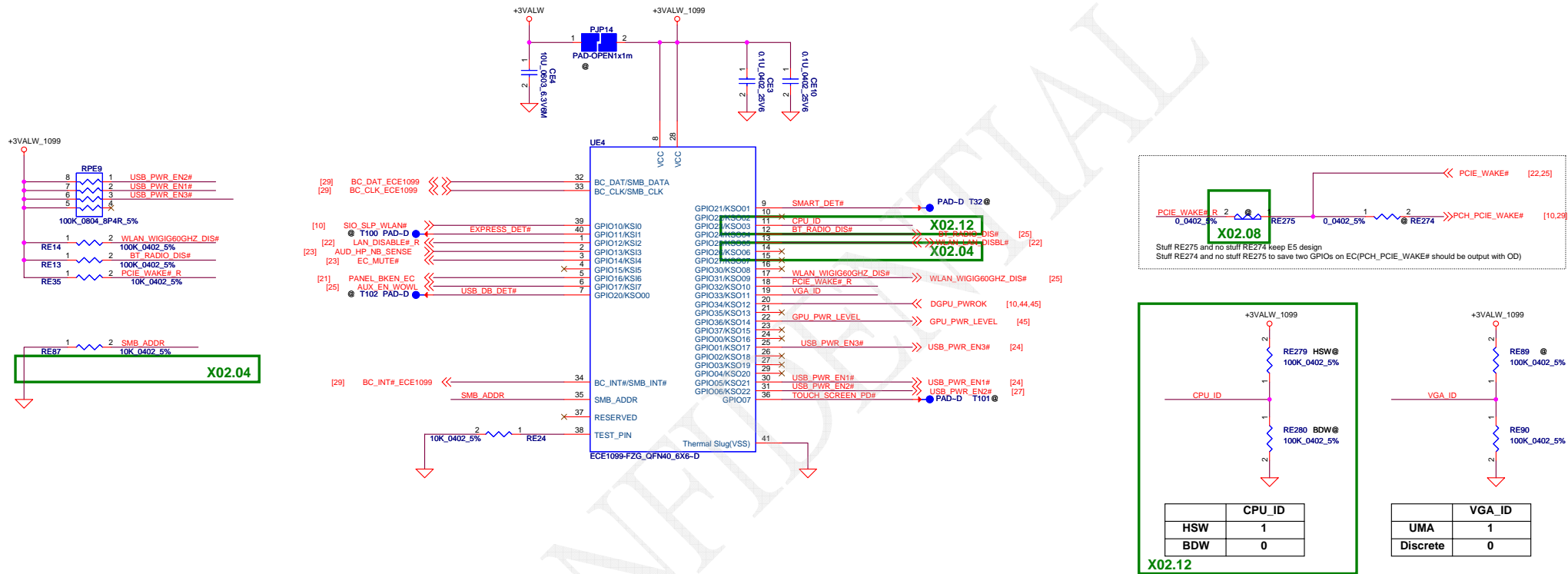
FAN

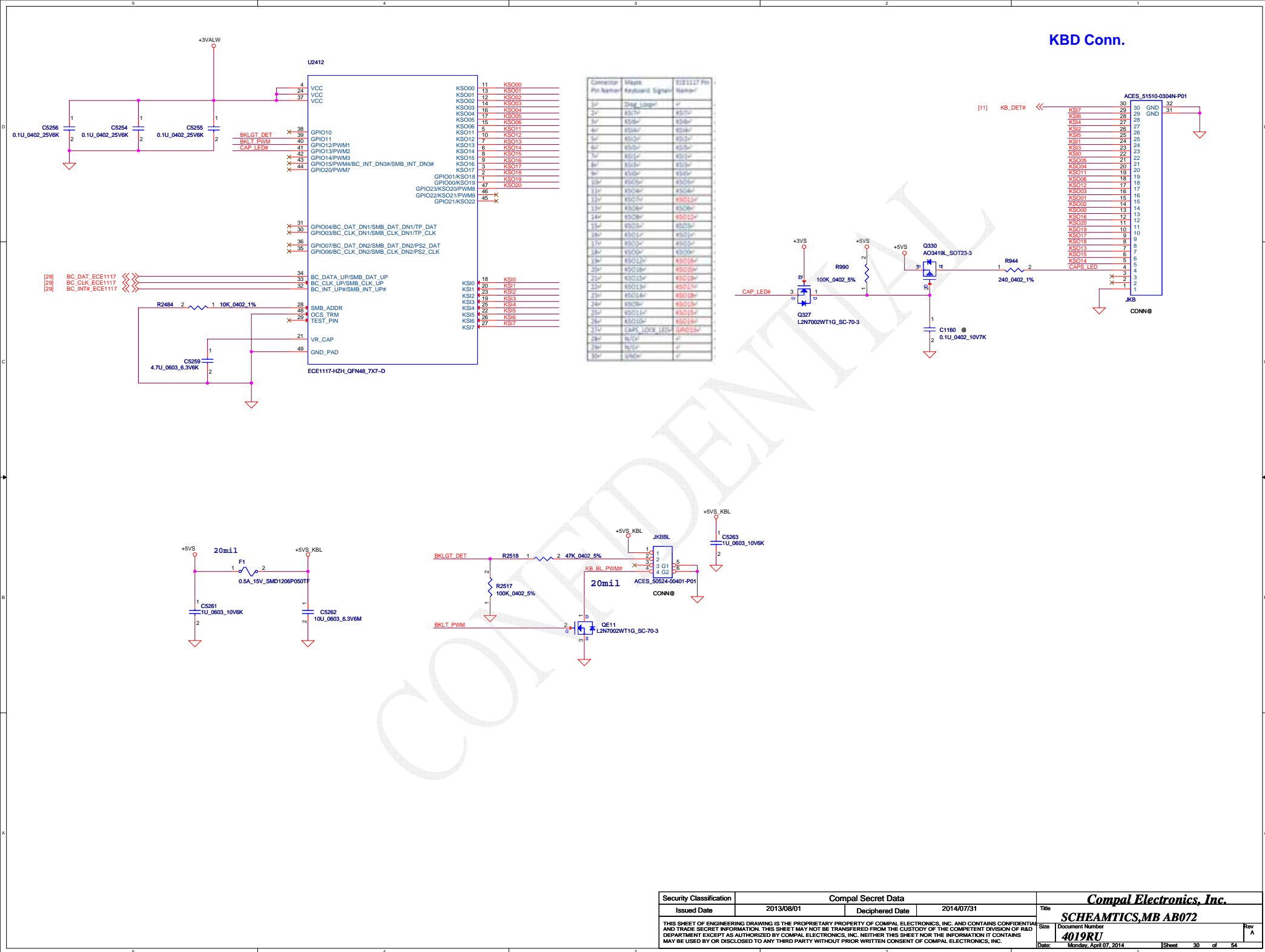


Touch pad



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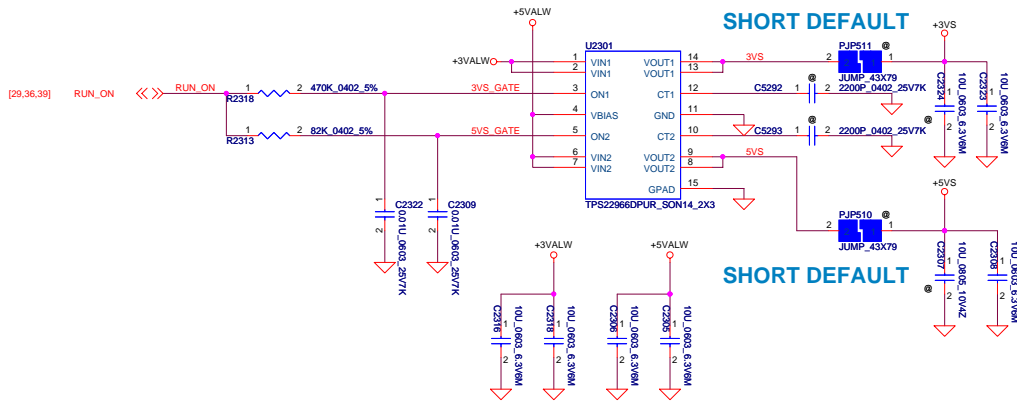




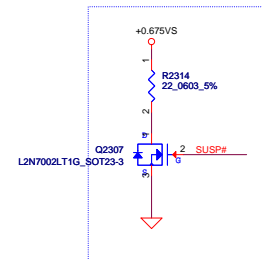
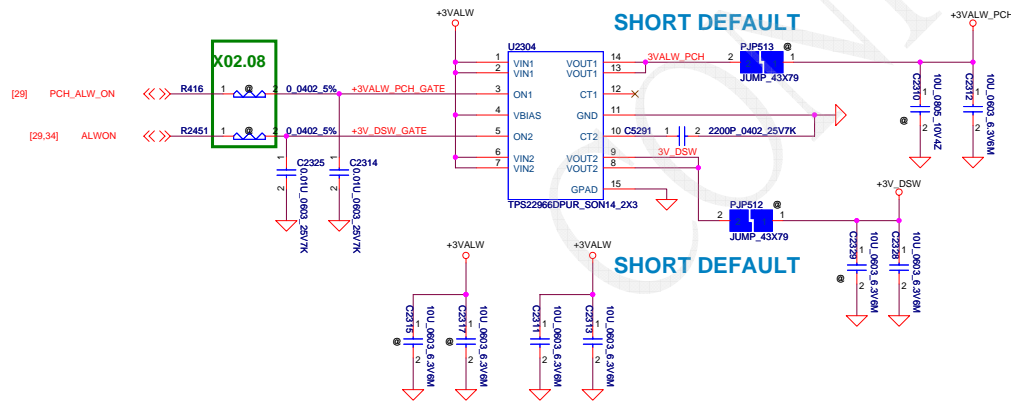
KBD Conn.

Connector	Pin Name	Maple	Keyboard	Signal	U2412 Pin
14P	KB_DET	KB_DET	KB_DET	KB_DET	11
2P	KB_DET	KB_DET	KB_DET	KB_DET	12
3P	KB_DET	KB_DET	KB_DET	KB_DET	13
4P	KB_DET	KB_DET	KB_DET	KB_DET	14
5P	KB_DET	KB_DET	KB_DET	KB_DET	15
6P	KB_DET	KB_DET	KB_DET	KB_DET	16
7P	KB_DET	KB_DET	KB_DET	KB_DET	17
8P	KB_DET	KB_DET	KB_DET	KB_DET	18
9P	KB_DET	KB_DET	KB_DET	KB_DET	19
10P	KB_DET	KB_DET	KB_DET	KB_DET	20
11P	KB_DET	KB_DET	KB_DET	KB_DET	21
12P	KB_DET	KB_DET	KB_DET	KB_DET	22
13P	KB_DET	KB_DET	KB_DET	KB_DET	23
14P	KB_DET	KB_DET	KB_DET	KB_DET	24
15P	KB_DET	KB_DET	KB_DET	KB_DET	25
16P	KB_DET	KB_DET	KB_DET	KB_DET	26
17P	KB_DET	KB_DET	KB_DET	KB_DET	27
18P	KB_DET	KB_DET	KB_DET	KB_DET	28
19P	KB_DET	KB_DET	KB_DET	KB_DET	29
20P	KB_DET	KB_DET	KB_DET	KB_DET	30
21P	KB_DET	KB_DET	KB_DET	KB_DET	31
22P	KB_DET	KB_DET	KB_DET	KB_DET	32
23P	KB_DET	KB_DET	KB_DET	KB_DET	33
24P	KB_DET	KB_DET	KB_DET	KB_DET	34
25P	KB_DET	KB_DET	KB_DET	KB_DET	35
26P	KB_DET	KB_DET	KB_DET	KB_DET	36
27P	KB_DET	KB_DET	KB_DET	KB_DET	37
28P	KB_DET	KB_DET	KB_DET	KB_DET	38
29P	KB_DET	KB_DET	KB_DET	KB_DET	39
30P	KB_DET	KB_DET	KB_DET	KB_DET	40
31P	KB_DET	KB_DET	KB_DET	KB_DET	41
32P	KB_DET	KB_DET	KB_DET	KB_DET	42
33P	KB_DET	KB_DET	KB_DET	KB_DET	43
34P	KB_DET	KB_DET	KB_DET	KB_DET	44
35P	KB_DET	KB_DET	KB_DET	KB_DET	45
36P	KB_DET	KB_DET	KB_DET	KB_DET	46
37P	KB_DET	KB_DET	KB_DET	KB_DET	47
38P	KB_DET	KB_DET	KB_DET	KB_DET	48
39P	KB_DET	KB_DET	KB_DET	KB_DET	49
40P	KB_DET	KB_DET	KB_DET	KB_DET	50
41P	KB_DET	KB_DET	KB_DET	KB_DET	51
42P	KB_DET	KB_DET	KB_DET	KB_DET	52
43P	KB_DET	KB_DET	KB_DET	KB_DET	53
44P	KB_DET	KB_DET	KB_DET	KB_DET	54
45P	KB_DET	KB_DET	KB_DET	KB_DET	55
46P	KB_DET	KB_DET	KB_DET	KB_DET	56
47P	KB_DET	KB_DET	KB_DET	KB_DET	57
48P	KB_DET	KB_DET	KB_DET	KB_DET	58
49P	KB_DET	KB_DET	KB_DET	KB_DET	59
50P	KB_DET	KB_DET	KB_DET	KB_DET	60

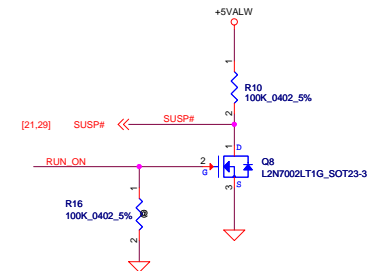
+5VS and +3VS switch



+3VALW_PCH switch

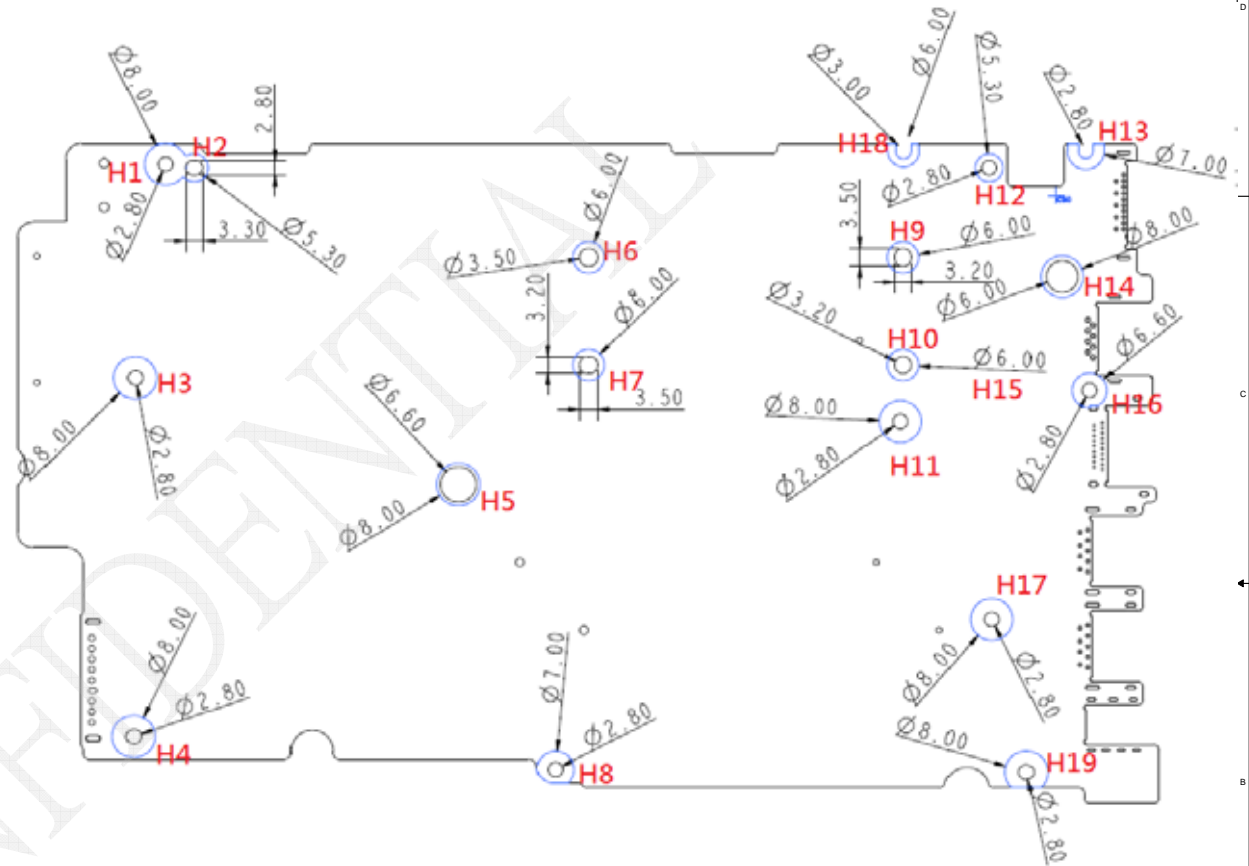
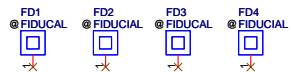
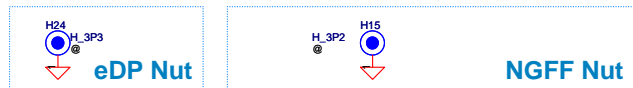
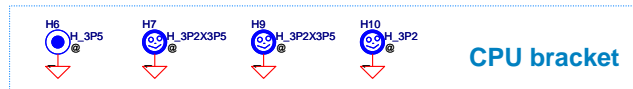
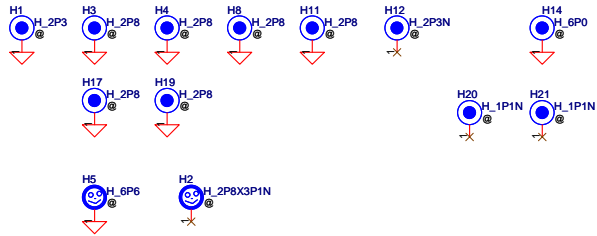


For Intel S3 Power Reduction



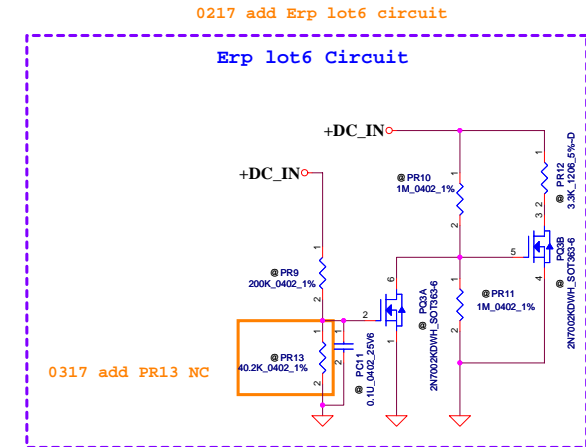
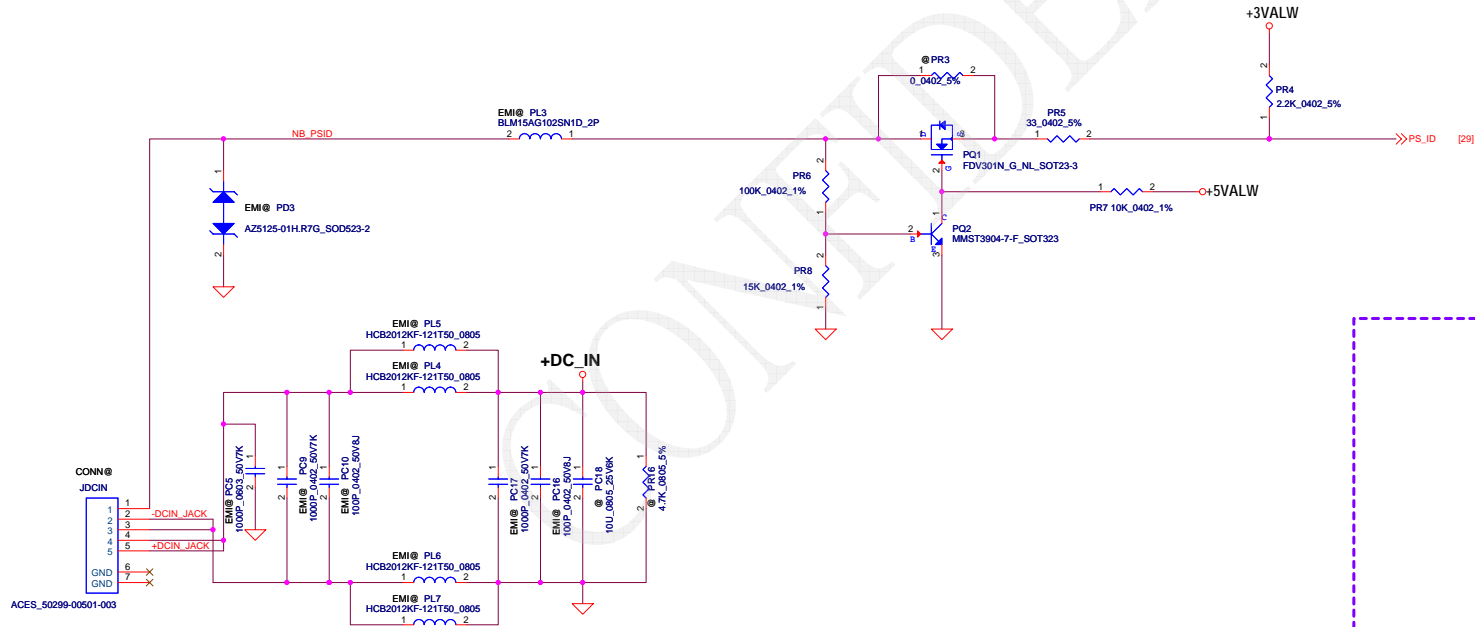
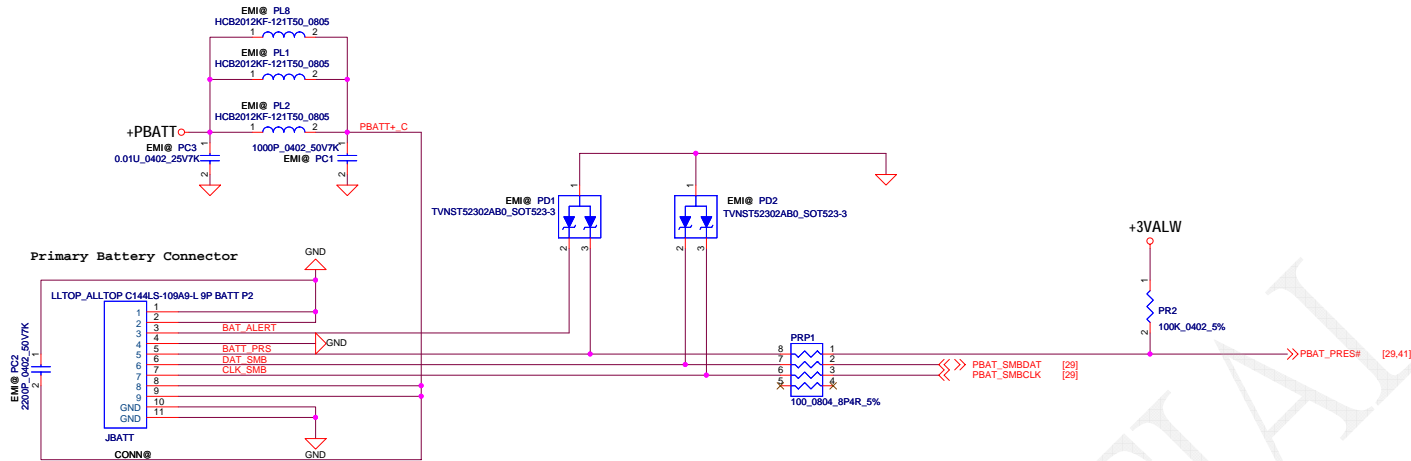
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Screw Hole



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SMART
Battery:
01.GND1
02.GND2
03.BAT_ALERT
04.SYS_PRES
05.BATT_PRS
06.DAT_SMB
07.CLK_SMB
08.BATT1+
09.BATT2+



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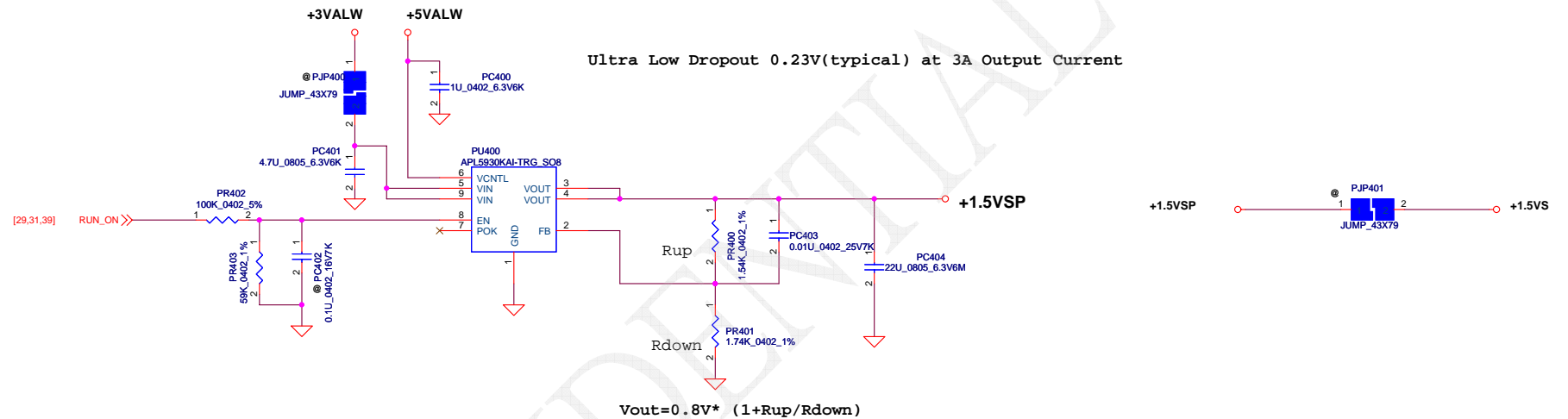


[0823] change DP to VGA solution, delet this design

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Module model information

APL5930_V1.mdd



1.5VS
TDC 0.014A
Peak Current 0.2A
OCP current 5.7A

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RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer

RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer

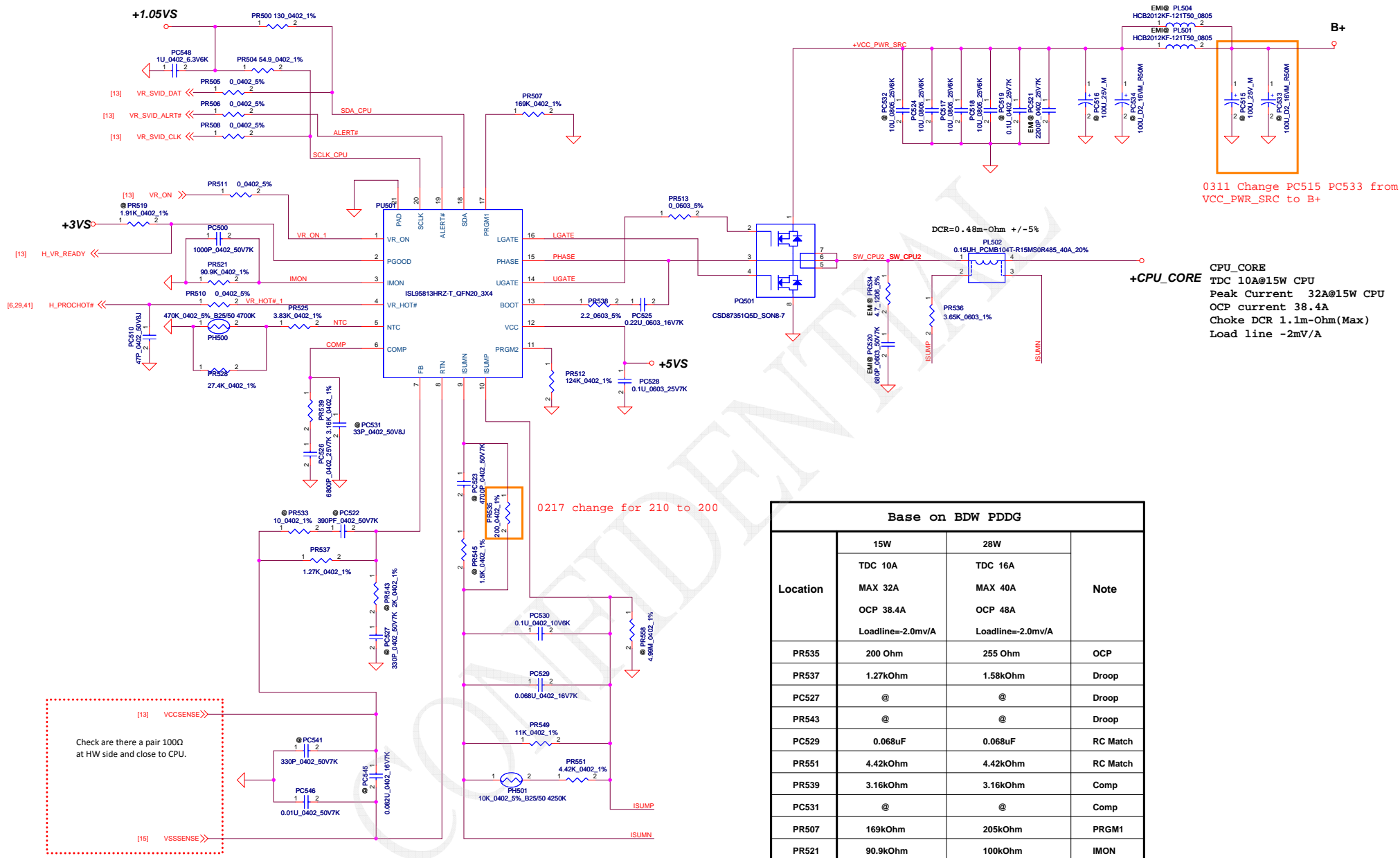
0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

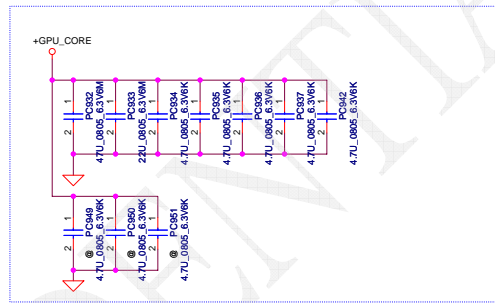


Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

1.35Volt +/- 5%
TDC 8.1A
Peak Current 8.4A
OCP 13.5A

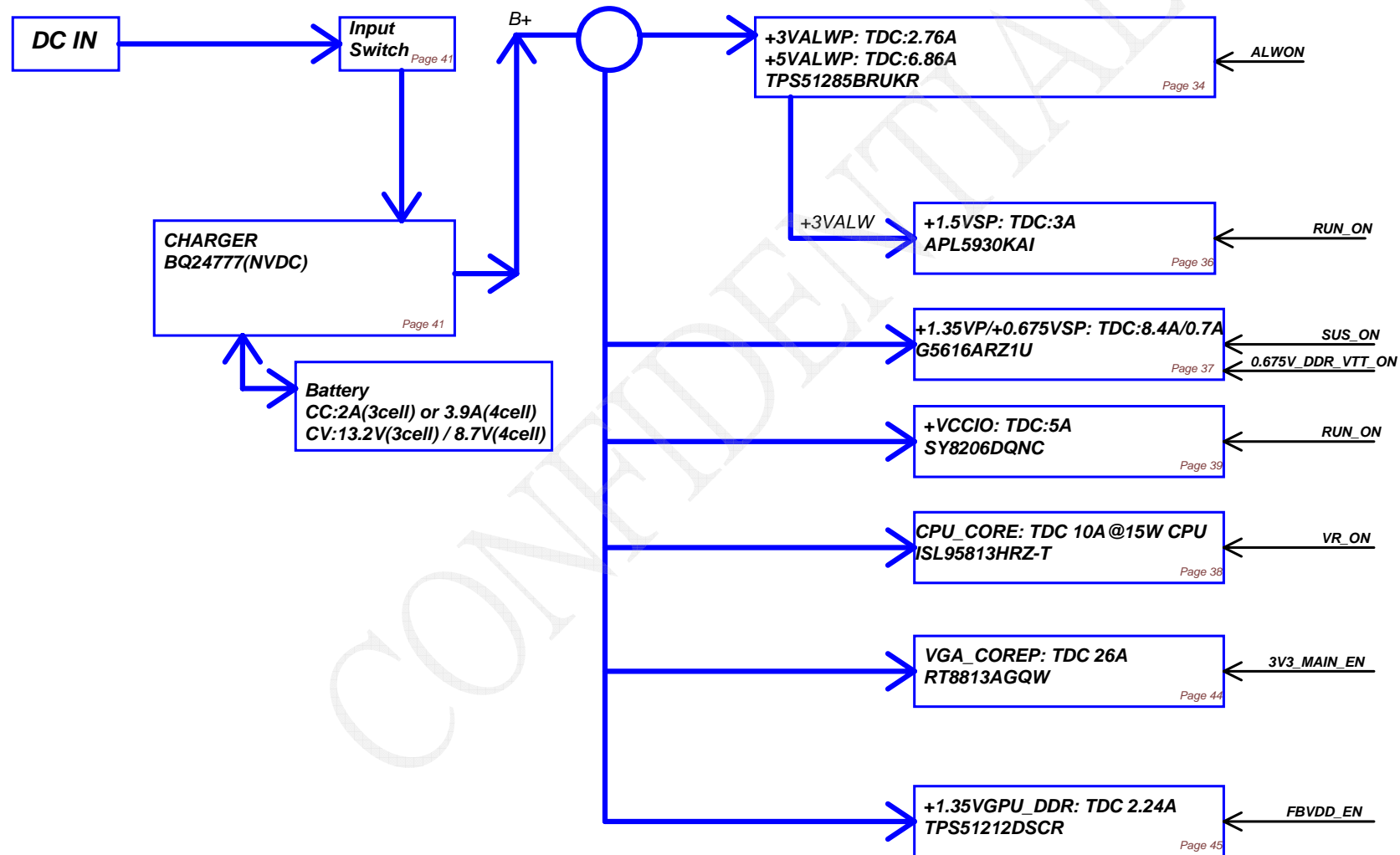
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nVidia GB2B-64 package
Near GPU
47uF 0805 *1
22uF 0805 *1
4.7uF 0805 *5

Power block



$V_{boot} = V_{vref} * R_{ref2} / (R_{ref1} + R_{ref2} + R_{boot})$
 $R_t = R_{refadj} // (R_{boot} + R_{ref2})$
 $V_{min} = V_{vref} * [R_{ref2} / (R_{ref2} + R_{boot})] * [R_t / (R_{ref1} + R_t)]$
 $V_{max} = V_{vref} * R_{ref2} / [(R_{ref1} // R_{refadj}) + R_{boot} + R_{ref2}]$
 $V_{out} = V_{min} + N * V_{step}$
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

PWM-VID Spec and component Values

PWM-VID Spec		Config A	Config B	Config C	
Vmin		0.6V	0.6V	0.65V	
Vmax		1.2V	1.2V	1.15V	
Vboot		0.875V	0.9V	0.9V	
Voltage step		6.25mV	6.25mV	25mV	
N of Voltage level		96	96	20	
Rref2=PR607+PR610	Rrefadj	PR604	39K	20K	39K
	Rref1	PR602	39K	20K	30K
	Rboot	PR603	1.5K	2K	3K
		PR607	30K	18K	24K
		PR610	1.5K	0	3K
C	PC607	1.5nf	2.7nf	1.8nf	

H-side MOS:MDU1516URH
 Rds(on):
 11.7mohm@Vgs=4.5V
 Id :18.6A@Ta=25 degC

L-side MOS:MDU1511RH
 Rds(on):
 2.7mohm@Vgs=4.5V
 Id :36.1A@Ta=25 degC

Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N15S-GM
OpenVReg Configurations	Config B
Rated TDP Power at Tj=102C	18W
Boosted GPU Total at Tj=102C	20W
EDP-Continuous at Tj=102C	22A
EDP-Peak at Tj=102C	48.11 A
Istep max (Evaluation)	29.22 A
OCF Setting Current	66A
Rocset	13K
Recommendation	2phase 1H1L
Polymer Cap (330uF)	9mohm * 3
Or OSCON (390uF)	NULL

PWM VID and Output voltage control
 1.Boot mode
 2.Standby mode (don't support)
 3.Normal mode

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

PSI Pull high on HW side

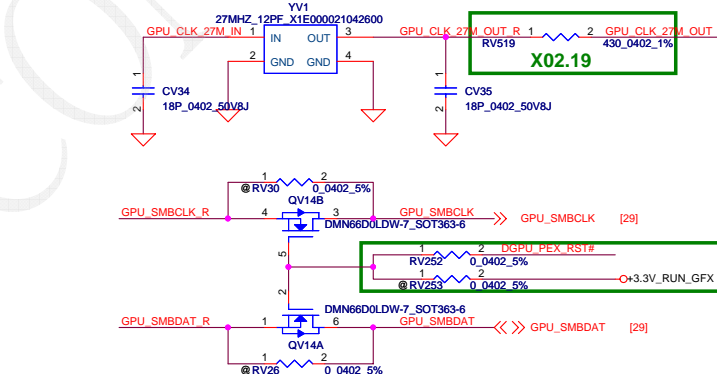
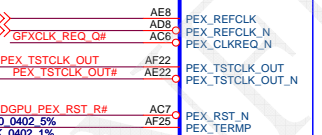
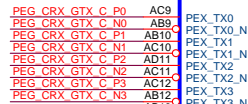
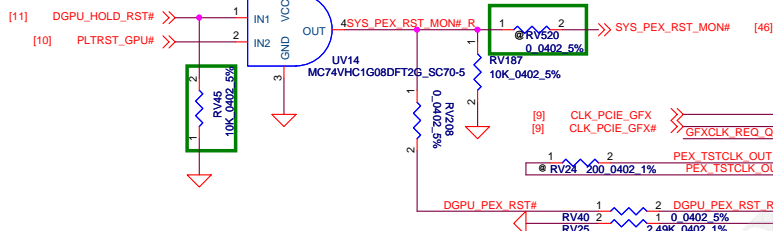
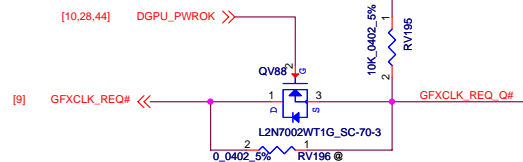
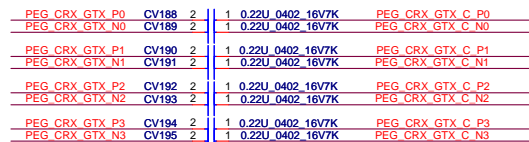
Pull high on HW side

Reserve Location

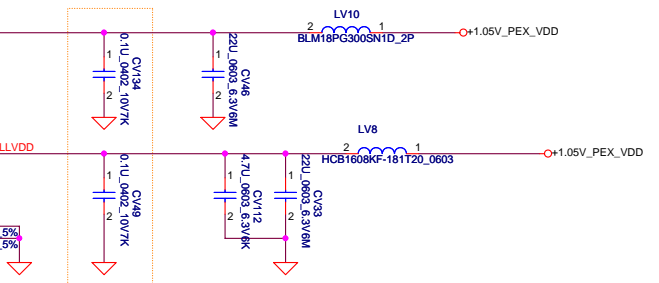
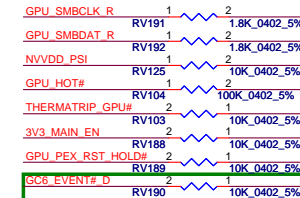
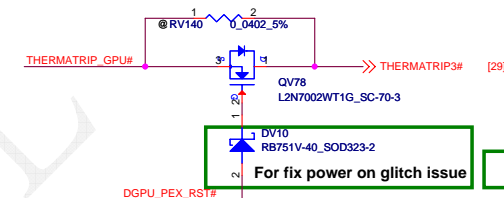
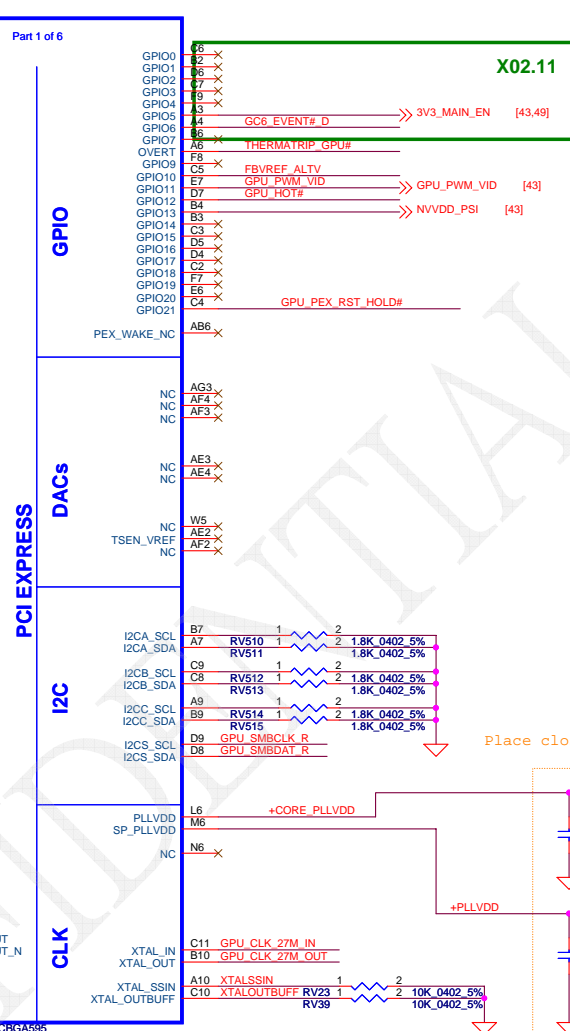
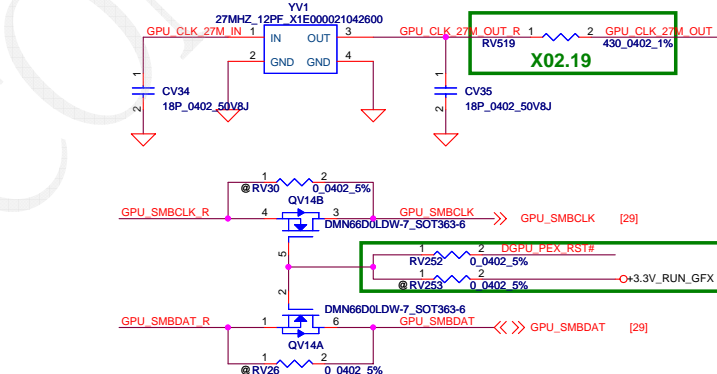
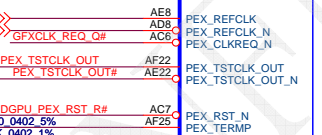
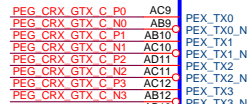
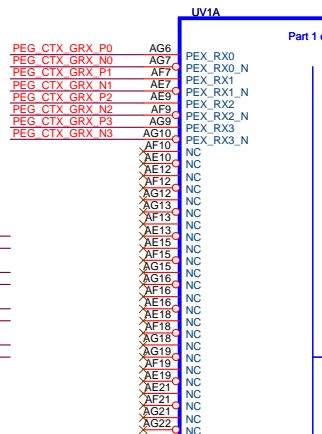
0217 PC604 change from pop to de-pop
 PC627 change from de-pop to pop

+VGA_CORE
 EDP-Continuous 22A
 EDP-Peak 48.11A
 OCP min 66A

- VSNS Soft-Start time (Internal) is 0.7ms (PC616 un-pop)
 $T_{ss} = (C_{ss} * V_{refin}) / I_{ss} + 2.3ms$
 $= 0.01uF * 0.9V / 5uA + 2.3ms = 4.1ms$ (PC616 pop)
- Switching frequency setting:
 $F_{sw} = (V_{in} - 0.5) / (2 * V_{in} * R_{ton} * 3.2p) = 304.89KHz$



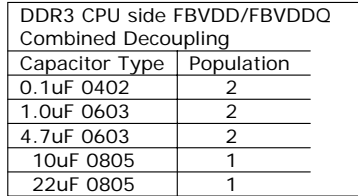
GPU_PWR_LEVEL	
LOW	Low Performace
HIGH	High Performace



Capacitor Type	Population
0.1uF 0402	1 per ball
4.7uF 0603	1
22uF 0805	1
Bead 180 ohm (ESR=0.2 ohm) 0603	1

PLL VDD Filtering	
Capacitor Type	Population
0.1uF 0402	1
22uF 0805	1
Bead 30 ohm (ESR=0.05 ohm) 0402	1

Re



PEX_PLLVDD Decoupling	
Capacitor Type	Population
0.1uF 0402	1
1uF 0603	1
4.7uF 0805	1

PEX_SVDD/PEX_PLL_HVDD Decoupling	
Capacitor Type	Population
0.1uF 0402	1
4.7uF 0603	2

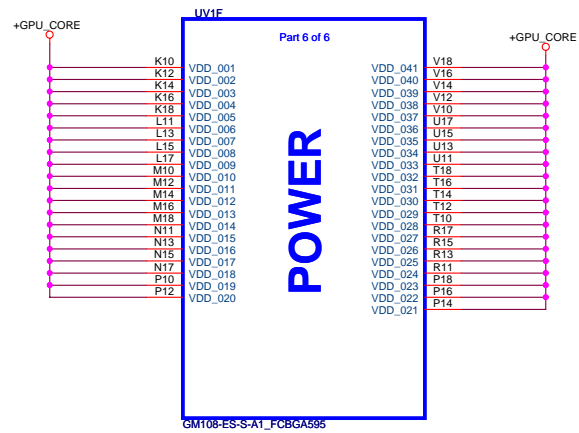
3V3_MAIN Decoupling	
Capacitor Type	Population
0.1uF 0402	2
1uF 0603	1
4.7uF 0603	1

3V3_AON Decoupling	
Capacitor Type	Population
0.1uF 0402	1
1uF 0603	1
4.7uF 0603	1

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Caps on Power Side
1UX4 4.7UX10 under GPU
4.7UX5 22UX1 47UX2 330UX2 near GPU



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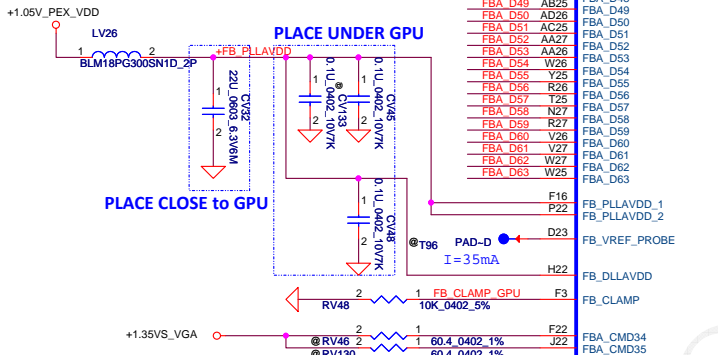
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Issued Date	2013/07/25	Deciphered Date	2014/07/24	Compal Electronics, Inc.	
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				4019RU	A
				Date: Monday, April 07, 2014	Sheet 48 of 54

GDDR3L CMD Mapping Table

DATA Bits[31..0] DATA Bits[63..32]

CMD0	CS0#	
CMD1	ODT	
CMD2	CKE	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE#	WE#
CMD14	A15	A15
CMD15	CAS#	CAS#
CMD16	CS0#	
CMD17		
CMD18	ODT	
CMD19	CKE	
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS#	RAS#
CMD31		

X02.11



FBx_PLL_AVDD and FB_DLL_AVDD Combined

Capacitor Type	Population
0.1uF 0402	2
22uF 0805	1
Bead 30 ohm (ESR=0.01 ohm) 0603	1



Part 2 of 6

MEMORY INTERFACE A

GM108-ES-S-A1_FCBGA595

FBA_D0 F18 FBA_D00

FBA_D1 F18 FBA_D01

FBA_D2 F18 FBA_D02

FBA_D3 F17 FBA_D03

FBA_D4 D20 FBA_D04

FBA_D5 D21 FBA_D05

FBA_D6 F20 FBA_D06

FBA_D7 E21 FBA_D07

FBA_D8 E15 FBA_D08

FBA_D9 D15 FBA_D09

FBA_D10 F15 FBA_D10

FBA_D11 F13 FBA_D11

FBA_D12 C13 FBA_D12

FBA_D13 B13 FBA_D13

FBA_D14 E13 FBA_D14

FBA_D15 D13 FBA_D15

FBA_D16 B15 FBA_D16

FBA_D17 C16 FBA_D17

FBA_D18 A13 FBA_D18

FBA_D19 A15 FBA_D19

FBA_D20 B19 FBA_D20

FBA_D21 A18 FBA_D21

FBA_D22 A19 FBA_D22

FBA_D23 C19 FBA_D23

FBA_D24 B24 FBA_D24

FBA_D25 C23 FBA_D25

FBA_D26 A25 FBA_D26

FBA_D27 A24 FBA_D27

FBA_D28 A21 FBA_D28

FBA_D29 B21 FBA_D29

FBA_D30 C20 FBA_D30

FBA_D31 C21 FBA_D31

FBA_D32 R22 FBA_D32

FBA_D33 R24 FBA_D33

FBA_D34 T22 FBA_D34

FBA_D35 R23 FBA_D35

FBA_D36 N25 FBA_D36

FBA_D37 N26 FBA_D37

FBA_D38 N23 FBA_D38

FBA_D39 N24 FBA_D39

FBA_D40 V23 FBA_D40

FBA_D41 V22 FBA_D41

FBA_D42 T23 FBA_D42

FBA_D43 U22 FBA_D43

FBA_D44 Y24 FBA_D44

FBA_D45 A24 FBA_D45

FBA_D46 Y22 FBA_D46

FBA_D47 AA23 FBA_D47

FBA_D48 AD27 FBA_D48

FBA_D49 AB25 FBA_D49

FBA_D50 AD26 FBA_D50

FBA_D51 AC25 FBA_D51

FBA_D52 AA26 FBA_D52

FBA_D53 D53 FBA_D53

FBA_D54 W26 FBA_D54

FBA_D55 R26 FBA_D55

FBA_D56 R26 FBA_D56

FBA_D57 T25 FBA_D57

FBA_D58 N27 FBA_D58

FBA_D59 V26 FBA_D59

FBA_D60 V27 FBA_D60

FBA_D61 V27 FBA_D61

FBA_D62 W27 FBA_D62

FBA_D63 W25 FBA_D63

F16 FBA_D64

P22 FBA_D65

D23 FBA_D66

H22 FBA_D67

F3 FBA_D68

F22 FBA_D69

J22 FBA_D70

F22 FBA_D71

J22 FBA_D72

F22 FBA_D73

J22 FBA_D74

F22 FBA_D75

J22 FBA_D76

F22 FBA_D77

J22 FBA_D78

F22 FBA_D79

J22 FBA_D80

F22 FBA_D81

J22 FBA_D82

F22 FBA_D83

J22 FBA_D84

F22 FBA_D85

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F22 FBA_D103

J22 FBA_D104

F22 FBA_D105

J22 FBA_D106

F22 FBA_D107

J22 FBA_D108

F22 FBA_D109

J22 FBA_D110

F22 FBA_D111

J22 FBA_D112

F22 FBA_D113

J22 FBA_D114

F22 FBA_D115

J22 FBA_D116

F22 FBA_D117

J22 FBA_D118

F22 FBA_D119

J22 FBA_D120

F22 FBA_D121

J22 FBA_D122

F22 FBA_D123

J22 FBA_D124

F22 FBA_D125

J22 FBA_D126

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F22 FBA_D165

J22 FBA_D166

F22 FBA_D167

J22 FBA_D168

F22 FBA_D169

J22 FBA_D170

F22 FBA_D171

J22 FBA_D172

F22 FBA_D173

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J22 FBA_D210

F22 FBA_D211

J22 FBA_D212

F22 FBA_D213

J22 FBA_D214

F22 FBA_D215

J22 FBA_D216

F22 FBA_D217

J22 FBA_D218

F22 FBA_D219

J22 FBA_D220

F22 FBA_D221

J22 FBA_D222

F22 FBA_D223

J22 FBA_D224

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J22 FBA_D228

F22 FBA_D229

J22 FBA_D230

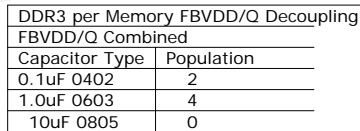
F22 FBA_D231

J22 FBA_D232

F22 FBA_D233

J22 FBA_D234

256x16 DDR3L



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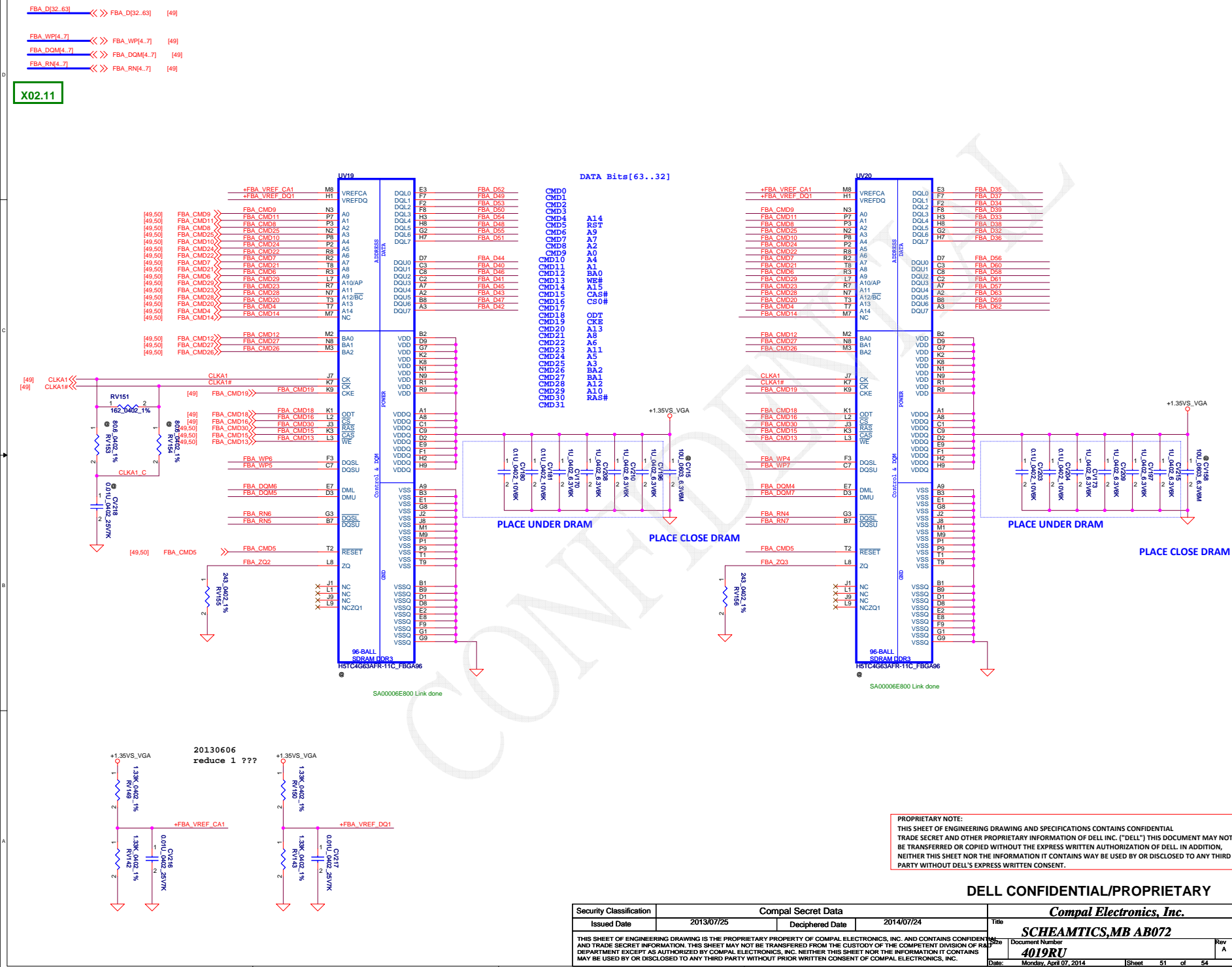
Document Number
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Memory Partition A - Lower 16 bits

256x16 DDR3L



Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	31	KB control	2013/10/21	EE	Change Fuse package for sales suggestion	Change F1 From SP040003E00 to SP040003A00	X01
2	23	Audio Codec ALC3234	2013/10/21	EE	fix POP noise issue	Add RAl129 from 100K to UAl pin 27, and NC RC366	X01
3	ALL	ALL	2013/10/21	EE	Re-name part of connector	JCRT1 --> JCRT, JAP51 --> JAPS, JDEG1 --> JDEG, JLPDE1 --> JLPDE, JKB1 --> JKB, JNGFF1 --> JNGFF JXDP1 --> JXDP, JRTC1 --> JRTC, PJPDC1 --> JDCIN, PBATT1 --> JBATT	X01
4	ALL	ALL	2013/10/21	EE	Re-name part of jump	PJ200 --> PJP200, PJ201 --> PJP201, PJ203 --> PJP203, PJ400 --> PJP400, PJ401 --> PJP401, JP12 --> PJP12 JP13 --> PJP13, JS10 --> PJP510, JS11 --> PJP511, JS12 --> PJP512, JS13 --> PJP513, PJ1000 --> PJP1000	
5	23	Audio Codec ALC3234	2013/10/23	EE	Update P/N for X1 code issue	Change LA8, LA9 form SM010018110 to SM01000E100	
6	1	Cover page	2013/10/28	EE	Add Micron sku for X76 level	Add UV17, UV18, UV19, UV20 for SA000077K0L, RV59 for 24.9K	X01
7	27	LED/DB	2013/10/29	EE	delete circuit for EC control LED blink issue	Delete Q2417	
8	29	KBC & GPIO MEC5085	2013/10/31	EE	Depop item by EC request	Depop RE278	
9	22	LAN RTL8111GUS-CG	2013/10/31	EE	Change Power switch for cost down plan	Change UL2 from SA00003AR00 to SA000079400, Delete CL38, Add RL41	X01
10	21	eDP/webcam/touch	2013/10/31	EE	Change Power switch for cost down plan	Change UX1, UX3 from SA00003AR00 to SA000079400, Delete CX9, CX52, Add RX30, RX31 to 100K	X01
11	31	DC/DC interface	2013/10/31	EE	Change Load switch for cost down plan	Change U2301, U2304 from SA00004MM00 to SA00006FD00	X01
12	50	N15S-MEM Interface A	2013/10/31	EE	Change Load switch for cost down plan	Change UV15 from SA00004MM00 to SA00006FD00	X01
13	25	NGFF_WLAN	2013/10/31	EE	Change Power switch for cost down plan	Change UM1 from SA00005XM00 to SA000070L00, Add CM8 to 2200P	X01
14	22	LAN RTL8111GUS-CG	2013/10/31	EE	Change Transformer for cost down plan	Change TL2 from SP050007Q00 to SP050006P00	X01
15	20	DP to CRT	2013/11/05	EE	Add cap for reduce power ripple by vendor confirm	Add CV361 to 22uF and close UV6 pin 38	X01
16	23	Audio Codec ALC3234	2013/11/05	EE	Add capacitor for codec stable	Add CA77 to 4.7uF_0603 and close UAl pin36	
17	19, 24, 26, 27	Common mode Choke	2013/11/12	EE	Change Common mode choke for X1 code	Change LI2, LX2, LI2, LX3, LX4, LX5, LI5, LX6, LX7, LI9, LI10 from SM070001S00 to SM070003Y00 Change LI1, LI3, LI4, LI6 from SM070001R00 to SM070003Q00	X01
18	27	LED/DB	2013/11/12	EE	Delete MB common mode choke by EA measure	Delete LI9, LI10	X01
19	46	N15S-PCIE	2013/11/13	EE	change bead for X1 code	Change LV8 from SM010028480 to SM010004700	X01
20	24, 27	USB	2013/11/13	EE	Change USB I/O power switch for Cost down	Change UI2, UI3, UI4 from SA00003XM00 to SA00007AO00, Delete CI7, CI14, CI18, CI45, Change CI6, CI12, CI44 from 4.7U_0805 to 1U_0603	
21	13, 17	Buffer output	2013/11/13	EE	change buffer output for cost down	Change UC6, U2303 from SA00005U600 to SA00007KJ00	X01
22	46	N15S-PCIE	2013/11/14	EE	change AND gate for cost down	Change UV14 from SA007080120 to SA00000OH00	X01
23	17, 27, 30	DDR & LED & KB	2013/11/14	EE	change MOSFET for cost down	Change Q12, QE11, Q327 from SB00000U000 to SB00000ST00, Change QD2 from SB501380050 to SB00000ST00	X01
24	23	Audio Codec ALC3234	2013/11/15	EE	modify by EMC request	Change RAl126, RAl127 to SM01000FG00, Change CA38, CA40 from 100p to 680p	X01
25	46, 50	N15S-PCIE	2013/11/15	EE	modify for GPU power sequence	Change RV45 from pull high to 45.3K pull down, Depop CV141, Change CV140 from 470P to 1000P	
26	23	Audio Codec ALC3234	2013/11/18	EE	Change EMI solution	Change RAl121, RAl122, RAl123, RAl124 from 0 ohm to SM01000NO00	X01
27	29	KBC & GPIO MEC5085	2013/11/18	EE	Add ESD diode by EMC request	Add DE2 for PE_CI_EC net	
28	26	HDD/Finger print	2013/11/19	EE	Rename Location	Re-name U2413 to DS1	
29	08, 29	Crystal	2013/11/20	EE	Crystal fine tune	Change CE53 from 22P to 27P	
30	20	DP to CRT	2013/11/21	EE	Add Power pin connect to power by vendor	Add RV518 10K to +3VS_VGA	
31	21	eDP/ HDD / PAD	2013/11/21	EE	change connector & PAD by ME	Change JEDP to SP010013I00, JHDD to SP02000TR00, H1, H2, H15, H24 update footprint	
32	23, 26	Audio & Finger	2013/11/21	EE	modify by EMC request	Change LA8, LA9 from SM010018110 to SM01000MJ00, Change RS39 from 0603 to 0402	
33	27	ESD	2013/11/21	EE	ESD BOM slim plan	Change DE1, DV5, DV6 to SCA00001L00,	
34	21	Camera	2013/11/21	EE	Camera voltage drop	Delete RX27, Add QX5 and Change +3VS to +3VALW	
35	23	Audio	2013/11/25	EE	Change ESD diode by EMC request	Change DA12 to SC400007Q00, Add DA14 to SC400007Q00	
36	46	N15S-PCIE	2013/11/26	EE	Add diode for prevent leakage	Add DV9 for GC6_EVENT#	
37	32	Screw Hole	2013/11/26	EE	Modify Screw hole by ME update DXF	Delete H13, H18, Add H24	
38	29	KBC & GPIO MEC5085	2013/11/27	EE	Change Connector for ME issue	Change JDEG from SP01001FF00 to SP01001LL00, Change JLPDE from SP01001FF00 to SP01000HE00	
39	21	eDP	2013/11/27	EE	Add EMI solution for eDP	Add LX8, LX9, LX10, for SM070003Q00, Add RX32, RX33, RX34, RX35, RX36, RX37 for 0 ohm	
40	29	KBC & GPIO MEC5085	2013/11/27	EE	Change Resistor for Thermal request	Change RE77 from 1.58K to 1.96K	
41	46	N15S-PCIE	2013/11/28	EE	GPU circuit modify by vendor feedback	Add RV519 for GPU_CLK_27M_OUT, pop DV8, RV29, reserve RV208, Change power for ROM_SO_GPU/ROM_SI_GPU/ROM_SCLK_GPU	

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42	24	USB3.0	2013/11/28	EE	Rename by EC request	Delete R11, connect UI2 to UE4 by USB_FWR_EN3#	X01
43	32	Screw Hole	2013/11/29	EE	Modify Screw hole by ME update DXF	Delete H16, Update H12 & H15	X01
44	23	Audio	2013/12/02	EE	Change EMC bead by EMC request	Change RA1126, RA1127 to LA10, LA11, P/N from SM01000FG00 to SM01000NA00, RC366 rename to RA1130	X01
45	19	HDMI	2013/12/02	EE	Update HDMI connector	Change JHDMI from DC232001500 to DC232001K00	X01
46	46	N15S-PCIE	2013/12/03	EE	fine tune crystal capacitor	Change CV34, CV35 from 10P to 18P	X01
47	22	LAN RTL8111GUS-CG	2013/12/03	EE	Change Wake on LAN fnction GPIO by EC request	Add R2532 for PCIE_WAKE# to LAN_WAKE#	X01
48	27	LED/DB	2013/12/04	EE	Change Tough PAD pin define for vendor request	Delete R2529, R2530, R2531 pull high, and change net CLK_TP_SIO/DAT_TP_SIO from pin1, pin2 to pin6, pin7	X01
49	26	HDD/Finger print	2013/12/04	EE	Update footprint by DFB request	Update JFP connector footprint	X01
50	27	LED/DB	2013/12/06	EE	Change Power button design for SMT issue	delete net from SW1 pin1 & pin4	X01
01	22	LAN	2014/02/10	EE	Update Jump name	Change JP3 to PJP3	X02
02	26	HDD	2014/02/10	EE	Update connector footprint for ME	Update JHDD connector	X02
03	08	RTC	2014/02/10	EE	Change crystal by Intel SPEC	Change YC1 from SJ100001K00 to SJ10000LT00	
04	27	LED	2014/02/10	EE	Change design by Dell request	Delete RZ24,Q12,RE21, change LED signal from SATA_ACT# to BREATHE_LED#, SATA_ACT# connect to RP37	
05	25	NGFF	2014/02/11	EE	Update CIS symbol for pin define correct.	Change UML from SA000070100 to SA000070S00	
06	21,27	MIC/Power Switch	2014/02/11	EE	Add ESD solution by EMC	Add DX4, DW1 for MIC_CLK/MIC_DATA, POWER_SW#_MB	
07	26	HDD	2014/02/25	EE	update circuit for 2nd source plan	Add RS40, RS41, RS42, RS43 for US2	
08	ALL	0 ohm to short pad	2014/02/25	EE	change footprint for 0 ohm cost down	Change RC43,RC44,RC45,RC46,RC57,RC59,RC126,RC37,RC40,RC41,RC42,RC47,RC55,RC78,RC81,RC97,RC107,R2355,R248,R250,R251,R257,R265,RV163,RV164,RV215,R2360,R2632,RM5,RM6,RS39,RE58,RE275,R416,R2451,RX32,RX33,RX34,RX35,RX36,RX37,RA1114,RA1115,RA1116,RA1117	
09	29	EC	2014/02/26	EE	Update EC Reversion resistor	Change RE79 from 130K to 62K	
10	23	AUDIO	2014/03/12	EE	Change footprint for cost down	Change CA23 from 0603 to 0402	
11	45-51	GPU	2014/03/04	EE	1. Update GPU circuit for GC6 feature change to pure Optimus function. 2. fine tune GPU power sequence	GC6 Function Changes: Delete DV8,DV29,DV9,DV8,RV29,DV9,QV86,CV363,RV181,QV87, Reserve RV520, Add RV51 pull high for SYS_PEX_RST_MON#. Use DGPU_FWR_EN to replace 3V3_MAIN_EN for +3V_RUN_GFX turn on time tuning. Delete DV4 and use GFX_CORE_PG to replace FBVDD_EN turn on +1.35VS_VGA. Change net name +3.3V_GFX_AON to +3.3V_RUN_GFX. Other Changes: Chang RV45 from 45K to 10K, De-pop RV31 as FAE recommend no use. Add DV10 solve DGPU_PEX_RST# turn on glitch issue. reserve CV140 for fine tune GPU turn-on-timing Add RE279,RE280 for CPU_ID pin	
12	28	EC	2014/03/05	EE	Add CPU_ID for HSW & BDW sku by EC request		
13	08	ME	2014/03/05	EE	Change ME switch for layout placemant	Change SW3 from SN200003E00 to SN200002Y00	
14	21	eDP	2014/03/07	EE	Fine tune B+ range	Change RX2 from 100K to 270K, Change RX3 from 100K to 47K	
15	27	FAN	2014/03/10	EE	Add ESD by EMC request	Add DE3 on FAN1_TACH/FAN1_PWM	
16	22	LAN	2014/03/12	EE	Remove jump for layout placement	Delete PJP3	
17	20	CRT	2014/03/12	EE	Remove 0 ohm for EMC request	Delete RV211,RV212,RV213	
18	29	EC	2014/03/12	EE	Update crystal for measure result	Change YE1 from CL=12.5pF(SJ100001K00) to 9pF(SJ100001A00)	
19	45	GPU	2014/03/12	EE	Update Resistor for measure result	Change RV519 form 0 ohm to 430 ohm	
20	20, 24, 26, 27	ESD	2014/03/13	EE	Update ESD diode footprint for ME height limit	Change DI2,DI5,DS1,DE1,DV5,DV6,DE3 from SCA00001L00 to SCA00001I00	
21	21	eDP	2014/03/14	EE	Change Capacitor for measure result	Change CX31 from 10V(SE102104K00) to 25V(SE00000G880), Change CV57 from Y5V(SE070104Z80) to X5R(SE00000G880)	
22	27	PWR Button	2014/03/17	EE	Change Footprint for layout require	Change SW1 footprint (the same P/N)	
23	13,17	MCP & DDR buffer	2014/03/18	EE	Change main source for IC issue	Change UC6, U2303 from SA00007KJ00 to SA00005U600	
24	29	Thermal	2014/03/18	EE	Reserve NGFF thermal sensor by Thermal team request	Reserve QE10	

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1	P40	PROCESSOR DECOUPLING	2013/11/12	PWR	SSI verify , Vcore keep 18 keep	PC901,PC907,PC923,PC912,PC903 change from pop to de-pop	
2	P41	Charger_BQ24777	2013/11/12	PWR	EMI requirement	Pc723,PC724,PC725 change from de-pop to pop	
3	P33	DCIN/BATT CONN/OTP	2013/11/12	PWR	EMI requirement	Add PL5/PL7(SM01000C000)	
4	P33	DCIN/BATT CONN/OTP	2013/11/12	PWR	EMI requirement	Add PL8(SM01000C000), PL1/PL2/PL5/PL6 change from SM010009C80 to SM01000C000 for finding 2nd source easily	
5	P33	VCORE	2013/11/12	PWR	EMI requirement	PL502 change from 0.22uH to 0.15uH	
6	P38	VCORE	2013/11/12	PWR	Vcore test result abjustmet value	PR521 change from 97.6k to 95.3k	
7	P38	VCORE	2013/11/12	PWR	change to Vendor (CYNTEC)	PL502 change to SH00000PQ00	
8	P38	VCORE	2013/11/12	PWR	EMI requirement	add PL504(SM01000C000)	
9	P38	VCORE	2013/11/12	PWR	for common part	PL501 change from SM010009C80 to SM01000C000	
10	P34	3.3VALWP/SVALWP	2013/11/13	PWR	for common part	PL100 change from SH00000MS00 to SH00000YC00	
11	P37	+1.35VP/0.675VSP	2013/11/13	PWR	for common part	PL200 change from SH00000KS00 to SH00000YE00	
12	P45	+1.35VGPU_DDR	2013/11/13	PWR	for common part	PL1001 change from SH00000MR00 to SH00000YV00	
13	P38	VCORE	2013/11/14	PWR	Vcore test result abjustmet value	PR521 change from 95.3k to 90.9k	
14	P39	+VCCIO	2013/11/15	PWR	for common part	PL302 change form SM010009C80 to SM01000C000	
15	P33	DCIN/BATT CONN/OTP	2013/11/21	PWR	ESD requirement	add PD3 (AZ5125-01H.R7G_SOD523-2)	
16	P34	3.3VALWP/SVALWP	2013/11/21	PWR	change to same material	PD101 change from SCA00002A00 to SCA00001W00	
17	P41	Charger_BQ24777	2013/11/21	PWR	peak shift issue	Add PQ709	
18	P44	VGA_COREP	2013/11/21	PWR	ocp modify to 66A	PR615 change from 10.7k to 13k	
19	P38	VCORE	2013/11/25	PWR	current rating issue	PC520 change from 0402 to 0603	
20	P41	Charger_BQ24777	2013/11/26	PWR	check circuit modify error	PQ708A swap pin1 and pin6	
21	P39	+VCCIO	2013/11/28	PWR	for buyer suggest change material	PR303 chang from SD00001FX00 to SD013000080	
22	P43	Charger_BQ24777	2013/11/28	PWR	Vendor spec BQ24777_REGN modify to 5.4V	R715 change from 121k to 154k	
23	P38	VCORE	2013/12/04	PWR	DFB issue	remove PL503	
24	P41	Charger_BQ24777	2014/2/17	PWR	peak shift issue	PR729 NC	
25	P41	Charger_BQ24777	2014/2/17	PWR	PIN21 change from NC to input current limit mode	add PR706 10Kohm and pull high	
26	P41	Charger_BQ24777	2014/2/17	PWR	leakage current issue	change PD701(SCS00003800) to PD702,PD703(SCS0340L010)	
27	P41	Charger_BQ24777	2014/2/17	PWR	PIN9 change from Voltage monitor to current monitor	change PC753(100P) to PR732 (20K)	
28	P38	VCORE	2014/2/17	PWR	Vcore test result abjustmet value	PR535 change from 210 to 200	
29	P43	VGA_COREP	2014/2/17	PWR	ME Z-High issue	PC604 change from pop to de-pop,PC627 change from de-pop to pop	
30	P33	DCIN/BATT CONN/OTP	2014/2/17	PWR	hiccup mode issue	add Erp lot 6 circuit	
31	P41	Charger_BQ24777	2014/2/21	PWR	plug Adapter system no work issue	add PR741 connect PQ709 Gate to GND	
32	P44	+1.35VGPU_DDR	2014/3/4	PWR	for EE suggest	net name change from FBVDD_EN to GFX_CORE_PG	
33	P41	Charger_BQ24777	2014/3/5	PWR	acoustic noise	add PC730,PC731,PC732 to de-pop	
34	P41	Charger_BQ24777	2014/3/11	PWR	Follow Houston test summary solution NC	PQ708A,PQ708B NC	
34	P38	VCORE	2014/3/11	PWR	acoustic noise	Change PC515 PC533 from VCC_PWR_SRC to B+	
35	P37	+1.35VP/0.675VSP	2014/3/14	PWR	select the correct voltage to 2.5V	PC214 change from SF000003000 to SF000003100	
36	P33	DCIN/BATT CONN/OTP	2014/3/17	PWR	hiccup mode issue	add PR13 NC	
37	P34	3.3VALWP/SVALWP	2014/3/17	PWR	Co-Lay	add PC116 PC117 NC	
38	P41	Charger_BQ24777	2014/3/17	PWR	follow TI solution	change PR725 from 100K to 1K	
39	P41	Charger_BQ24777	2014/3/21	PWR	hiccup mode issue	change PR739 from 316K to 294K	
40	P34	3.3VALWP/SVALWP	2014/3/24	PWR	follow EC solution	PR110 NC	

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